64000 LOGIC DEVELOPMENT SYSTEM

Service

MODEL 64940A
TAPE CONTROL AND DRIVE

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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SERVICE MANUAL

MODEL 64940A

TAPE CONTROL AND DRIVE

REPAIR NUMBERS

This manual applies directly to PC boards with repair numbers prefixed 1923A. For additional information about repair numbers, refer to INSTRUMENTS COVERED BY THIS MANUAL in Section I.

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION

1-2. This manual contains technical information concerning the operation, maintenance, troubleshooting and theory-of-operation of the 64940 Cartridge Tape System as used in the 64000 Logic Development System. A point of particular interest to service personnel is the maintenance philosophy of repairing the Tape Controller PCB to the chip level but replacing the Tape Transport (together with its associated record/playback electronics) as a complete unit if it malfunctions. Therefore, there are no detailed descriptions of this latter unit in this manual.

1-3. This manual is organized into eight sections: Section 1 introduces the reader to this manual and gives a brief physical description of the Cassette tape system. Section II presents the installation and removal procedures for the tape system components. Section III covers operation and handling. Section IV describes how to troubleshoot and repair the cassette system while Section V discusses preventative maintenance procedures. Section VI lists the replaceable parts and Section VII contains backdating information needed to make this manual applicable to older machines. Section VIII presents the theory-of-operation of the cassette system and is intended to support the troubleshooting procedures.

1-4. DESCRIPTION

1-5. The 64940 Tape System consists of two basic assemblies: 1) the 64940-66501 Tape Controller PC Board and 2) the 98075A Tape Transport (see Figure 1-1). The Tape Controller PC Board plugs into a cardcage slot of the 64100A Mainframe. Normally, the Tape Controller PC Board is plugged into slot "0" behind the three system PCAs; however, it can be plugged into any of the available motherboard expansion card slots if desired.

1-6. The 98075A Tape Transport mounts to the inside front of the 64100 Mainframe bezel, to the right of the CRT. This allows the operator easy access to the tape system. The Tape Transport is connected to the Tape Controller PC Board via a keyed, 20-conductor ribbon cable.

1-7. The 64940A option is comprised of the following items:

1. Tape Transport ..... HP P/N 98075A
2. Tape Controller PC Board ... HP P/N 64940-66501
3. Flex Cable (Control) ..... HP P/N 64940-61601
4. Front Panel ..... HP P/N 5041-1532
5. Tape Cartridge ..... HP P/N 5061-3660

6. Flex Cable (I/O Bus) ..... HP P/N 64940-61602

NOTE

The 5061-3660 tape cartridge has replaced the 9162-0061 cartridge as of October, 1979.

1-8. APPLICATION

1-9. The 64940 Cartridge Tape System is available as an option to the 64100 Logic Development Station. Since the 64000 System software programs are contained on the 64800A and 64840A system cartridges, there must be at least one tape system for every 64000 System cluster of work stations. There can also be the possibility of a tape system for each work station in the cluster.

1-10. The Cartridge Tape System has three typical applications: 1) to load the system software onto the disc drive used with the 64000 System, 2) for file backup, and 3) the tape system allows files to be transferred from one system disc to another.

NOTES

1. The cassette tape system provides the only means of loading the 64000 Logic Developement System software onto the mass storeage disc.

2. All important program files and data files should be backed-up on cassette tape in the event of a disc failure.

1-11. SPECIFICATIONS

1-12. The following list of specifications define some of the basic characteristics of the cassette tape system:

Read/Write Speed	22 ips
Search/Rewind Speed	90 ips
Mini-cartridge Capacity	250 Kbytes
Maximum number of files	128 files
Information Format	HP Standard Interchange Format (SIF)

1-13. SAFETY CONSIDERATIONS

1-14. There are no safety hazards associated with the Model 64940A since there are no high voltages present. There are, however, high voltages associated with the 64100A Mainframe and appropriate warnings are given where some hazzard may be present.

1-15. INSTRUMENTS COVERED BY THIS MANUAL

1-16. This manual covers only the 64940A Cassette Tape System as used in the 64000 Logic Development System. It does not apply to other versions of this system used in other applications.

1-17. Attached to the instrument is a repair number tag. This 10-digit number is in the form: 0000A00000. The first four numbers and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and thus uniquely identifies each instrument. The contents of this manual apply mainly to instruments whose repair number is listed on the title page. However, backdating information is presented in Section VII to cover earlier instruments.

1-18. An instrument manufactured after the printing of this manual may may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument will be accompanied by a "Manual Changes" supplement. This supplement will contain change information that explains how to adapt this manual for the newer instrument.

1-19. In addition to change information, the supplement will contain information for correcting errors in this manual. To keep this manual as current as possible, Hewlett-Packard recomends that you periodically request the latest manual changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-20. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Office.

1-21. RECOMMENDED TEST EQUIPMENT

1-22. Equipment required to test and maintain the Model 64940A is listed in Section IV of this manual.

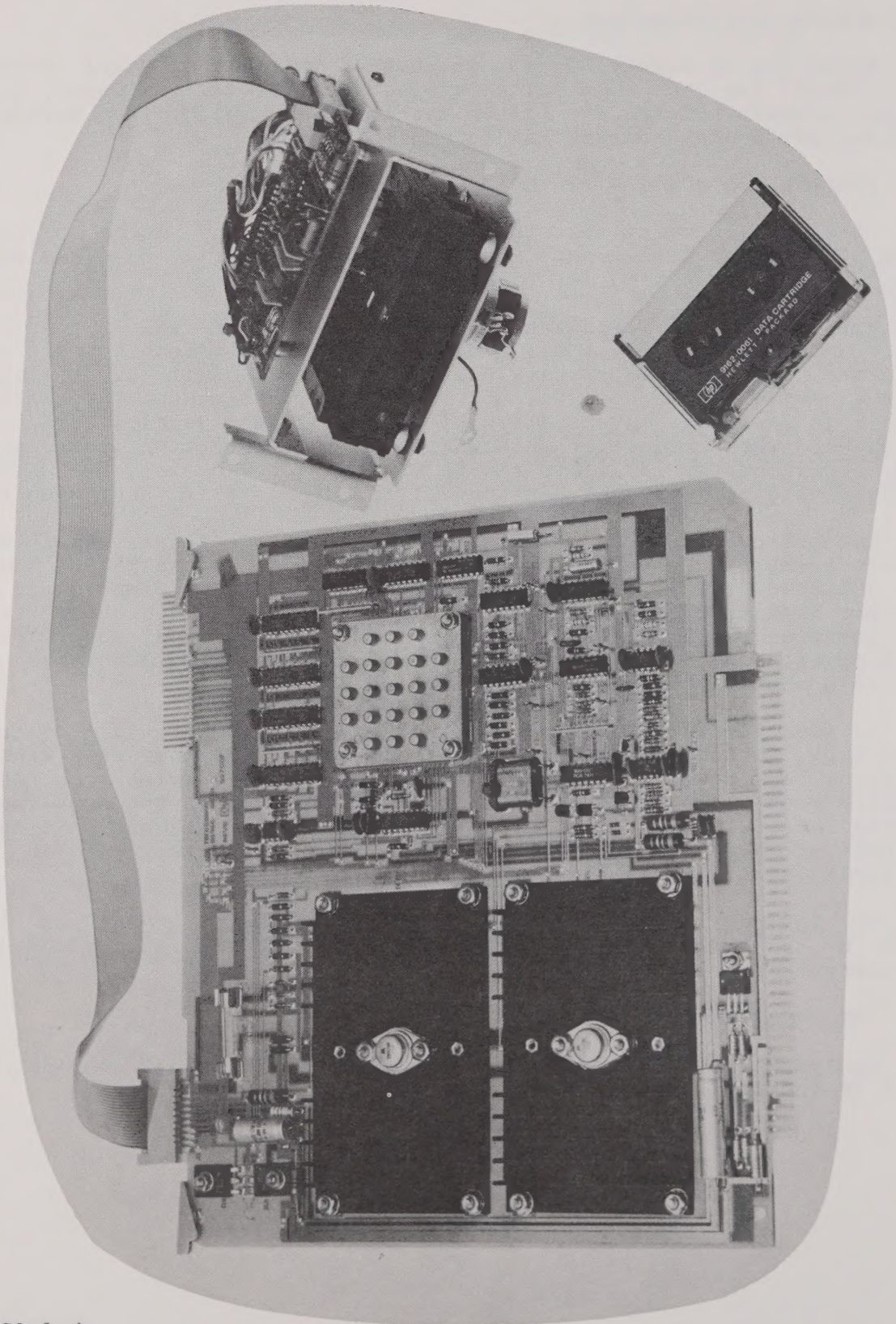

Figure 1-1. Tape Controller PCB and Transport Assy.

SECTION II

INSTALLATION AND REMOVAL

2-1. INTRODUCTION

2-2. This section describes the installation and removal procedures for the Controller PC board and the Tape Transport.

2-3. TAPE CONTROLLER PC BOARD

2-4. REMOVAL. To remove the Tape Controller PC Board:

a) Shut off system power and remove the card cage access cover.

b) Remove the 20-pin ribbon cable interconnecting the Tape Transport to the Tape Controller PC Board.

c) Remove the 50-pin ribbon cable interconnecting the Tape Controller PC Board to the I/O bus.

d) Pull up on removal extractors on top left and right sides of the controller board until it can be removed from the motherboard slot.

2-5. INSTALLATION. To install the Tape Controller PC Board, perform the removal steps in reverse order. However, be certain that the Tape Controller PC Board is properly centered in the motherboard connector before seating the board.

****
CAUTION
****
Do not force the PC board into the motherboard connector.

2-6. TAPE TRANSPORT

2-7. REMOVAL. To remove the Tape Transport Assembly:

a) Shut off system power and remove the entire top cover.

b) Remove the 20-pin ribbon cable interconnecting the Transport Assembly to the Tape Controller PC Board.

c) Remove the two hold-down screws on each side of the CRT front panel.

d) Tilt the front of the CRT display forward on its hinges.

****
* WARNING *
****

The CRT interconnecting wiring may contain hazardous voltages even with the main power switch in the OFF position. Therefore, use extreme care when tilting the CRT display forward so that the CRT interconnecting cables are not strained or damaged.

e) Remove the four screws from corners of transport mounting frame.

f) Remove transport from mainframe front panel.

NOTE

Repair of the transport assembly is supported to the module level only. To replace transport, remove the mounting hardware from failed transport and install on the replacement transport.

2-8. INSTALLATION. To install the tape transport, perform the removal steps in reverse order. Ensure that the mounting hardware is properly installed on the replacement tranport.

SECTION III

OPERATION

3-1. GENERAL

3-2. To operate the tape system it is necessary only to insert a tape cartridge through the door on the front panel of tape transport. All data transfers are performed via operator instructions executed from the keyboard of the 64100 Mainframe.

****
CAUTION
****

When inserting the cartridge into the transport, there is no need to push hard. Use of too much force may result in a "Servo Fail" error message.

3-3. The indicator light (located next to the tape cartridge eject button) is "ON" whenever the tape is moving.

****
CAUTION
****

Do not remove the tape cartridge while the "moving" indicator is on. This could result in damage to the information stored on the tape.

3-4. Information on the tape may be protected from being overwritten (write protected), by moving the "record" tab (on the cassette cartridge) away from the record position. If the cartridge is write protected when a write operation is attempted, the "write protected" error message will be displayed.

3-5. TAPE CARTRIDGE HANDLING

3-6. Dust and dirt are by far the greatest causes of cartridge related errors. Several basic precautions can reduce such problems:

a) Clean the tape head and capstan (drive wheel) of the Tape Transport after every 5 to 8 hours of use (more frequently in dirty environments).

b) Keep the Tape Transport door clean.

c) Keep the cartridge in the plastic container supplied when not in use.

d) Frequently condition (i.e., unwind and rewind) the tape to allow for even tension during read/write operations (see "Checksum Error" paragraph at end of this section).

3-7. Two other factors can affect the reliability of the tape cartridge: 1) strong magnetic fields can erase data and programs stored on the cartridge, and 2) physical damage to the tape, such as wrinkled or folded tape, can also cause record or load problems. A backup copy should always be maintained of all critical programs.

****
CAUTION
****

Avoid placing a tape cartridge on top of the disc drive used with the 64000 System. The strong magnetic field produced by the disc may damage or cause loss of data on the tape cartridge.

3-8. TAPE SYSTEM ERRORS

3-9. During normal system operation of the tape unit, there are two types of errors: fatal errors and non-fatal errors.

3-10. NON-FATAL ERRORS. These errors do not terminate the current software operation; they only give an error message and continue the operation. Two or more non-fatal errors occurring on the same file will result in only the higher priority error being displayed. Non-fatal errors include:

PRIORITY	ERROR MESSAGE	MEANING
5	FMGR Error	File Manager Software
	End of File	(Self Explanatory)
	Illegal Disc	" "
	File Not Found	" "
	File Already Exists	" "
	Disc Full	" "
	Directory Full	" "
	Corrupt File	" "
4	File Not on Cartrdige	" "
3	Checksum Error	Data Unreadable
2	Files Not Identical	Cannot be Verified
1	Low Threshold Required	Marginal Signal

3-11. FATAL ERRORS. These errors terminate the software operation. This action requires the operation to be re-initiated by the operator. Fatal errors include:

1. Cartridge Out
2. Power Fail
3. Tape Cartridge Hardware Not Present
4. Servo Failure
5. Device Timeout
6. Illegal Directory or Tape Format
7. FMGR Error While Listing File
8. Write Protected

3-12. CHECKSUM ERRORS. If a "checksum" error is encountered, the first step towards troubleshooting should be to condition the tape. Conditioning (re-tensioning) a tape is done by winding the tape to the end and then rewinding it back to the beginning. The keyboard actions are:

Type "tension" then press RETURN

3-13. Conditioning is necessary for smooth, continuous operation of the cartridge. If a checksum error occurs after conditioning, check the tape system for dirty heads or other transport problems. If the tape is the cause of the problem, it will be necessary to regenerate the tape.

3-14. STATUS MESSAGES

3-15. During normal operation of the tape system, status messages will be presented on the status line of the CRT display. Status messages include:

1. Storing File
2. Restoring File
3. Verifying File
4. Searching
5. Rewind
6. Reading Directory
7. Writing Directory
8. Pre-marking Directory
9. Store Complete
10. Restore Complete
11. Verify Complete
12. Waiting for Input
    a. "Insert New Tape"
    b. (File) "Already Exists", "Delete Old?"

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SECTION IV

PERFORMANCE VERIFICATION AND TROUBLESHOOTING

4-1. PERFORMANCE VERIFICATION (PV)

4-2. GENERAL. The 64940 Cartridge Tape System is exercised by a software routine that tests every function of the tape system. The Tape Test Performance Verification tests (PV) are a subroutine of the 64100 Mainframe PV and includes Signature Analysis (SA).

4-3. The following areas and functions of the tape system are tested by the Tape Test PV:

1. Hole Detectors (Transport)
2. High Speed Reverse
3. High Speed Forward Search (High Velocity Flux/Gap Detect)
4. Normal Speed Forward and Reverse
5. Write Data and Gap
6. Read Data and Gap
7. Servo Fail Detect
8. "Cartridge In" Switch (Transport)
9. "Record" Switch (Transport)
10. Powerfail Detect (External Software)

4-4. PV TEST SEQUENCE. When executing the PV, the following sequence is performed:

1. Rewind tape to load point
2. Write I.D. file on track 0
3. Write data file on track 0
4. Write end of valid data gap on track 0
5. Rewind tape to load point
6. Write I.D. 1 file on track 1
7. Write data 1 file on track 1
8. Write I.D. 2 file on track 1
9. Write data 2 file on track 1
10. Write end of valid data gap on track 1
11. Rewind tape to load point
12. Read data file on track 0 and compare
13. Rewind tape to load point
14. Search track 1 for data 2 file
15. Read data 2 file on track 1 and compare
16. Start again at beginning

4-5. When executing the cartridge tape system PV, it is important to associate the particular test that has failed with the displayed error message. Table 4-1 is a list of the error messages that can be encountered. With each message is a list of functional areas that may have failed. This list is not totally complete and thus should be used only as a guide.

Table 4-1. TAPE SYSTEM ERROR MESSAGES

MESSAGE	POSSIBLE AREA OF FAILURE	INVOLVED MODULE
1. Powerfail	1. Power Supply or 115 vac Line	Mainframe
2. Cart. out	1. Cart. not inserted properly	Transport
	2. Bad transport	Transport
	3. Bad TACO chip U9/gasket	Controller PCB
	4. Bad transport cable	Xport/Cont PCB
3. Servo Fail	1. Cart. inserted too hard	Cart/Xport
	2. Servo circuit failure	Controller PCB
	3. Motor failure	Transport
	4. Tachometer circuit failure	Xport/Cont PCB
	5. Servo fail detection ckt.	Controller PCB
	6. Bad TACO chip U9/gasket	Controller PCB
	7. Bad transport cable	Xport/Cont PCB
	8. Worn tape	Tape Cartridge
4. Write protected	1. Cartridge write protected	Tape Cartridge
	2. Bad transport	Transport
	3. Bad TACO chip U9/gasket	Controller PCB
5. Device Time Out	1. Bad transport	Transport
	2. Bad TACO chip U9/gasket	Controller PCB
	3. Motherboard buffer failure	Controller PCB
	4. Bad transport cable	Xport/Cont PCB
6. No Response Hardware	1. Cont. PCB not plugged-in	Mainframe
	2. Bad TACO chip U9/gasket	Controller PCB
	3. Motherboard buffer failure	Controller PCB
	4. Bad mainframe I/O cable	Mainframe
	5. Clock circuit failure	Controller PCB
7. End of Valid Data Found	1. Bad transport	Transport
	2. Bad TACO chip U9/gasket	Controller PCB
	3. Worn tape	Tape Cartridge
	4. Bad transport cable	Xport/Cont PCB
8. Read 2nd-4th try	1. Worn tape	Tape Cartridge
	2. Dirty head or bad transport	Transport
9. Checksum Error	1. Worn tape	Tape Cartridge
	2. Dirty head or bad xport	Transport
	3. Bad TACO chip U9/gasket	Controller PCB
10. Track Select Error	1. Bad TACO chip U9/gasket	Controller PCB
	2. Bad transport	Transport
	3. Bad transport cable	Xport/Cont PCB
11. No message on CRT	1. Initialize circuit failure	Controller PCB
	2. Bad TACO chip U9/gasket	Controller PCB

4-6. TROUBLESHOOTING

4-7. BASIC APPROACH. When troubleshooting a tape system failure, it is suggested that the following basic steps be performed in order to minimize the time required for isolating a particular failure.

4-8. If trouble is suspected, visually inspect the instrument and look for loose or burned components that might suggest a source of trouble. Verify that all circuit board connections are making good contact and are not shorting to an adjacent circuit. Attempt to complete the Performance Tests in this Section. If no obvious trouble is found, check the instrument power supply voltages and external line voltage before beginning extensive troubleshooting.

4-9. TROUBLE ISOLATION PROCEDURE:

a) 1. Shut off system power.
   2. Replug all involved connections.
   3. Reset system (power up).
   4. Check all supply voltages (+12, -12, -5, -6, and +17 vdc).
   5. Run PV (Tape System Test)

b) 1. Clean transport head.
   2. Install new tape cartridge (blank cartridge).
   3. Run PV.

c) Install spare transport and re-run PV.

d) 1. Install spare TACO chip (U9) and spare gasket and
   2. Re-run PV

e) Check operation of controller Clock circuit (See Figure 4-1).

f) Check operation of controller Initialization circuit (See Figure 4-1).

g) Do complete Signature Analysis tests (See "Signature Analysis" paragraph below).

h) Do analog "Servo test" on servo circuits and tachometer circuits (See "Servo Test" paragraph below).

4-10. SERVO TEST. This test allows troubleshooting the analog servo circuitry. During normal operation the servo circuitry is controlled under continuous feedback and is never in steady-state operation. Thus, the circuit waveforms are constantly varying which makes interpretation difficult. This test places the circuits into a steady-state cycle operation which allows inspection of signals at specific points throughout the servo loop.

4-11. EQUIPMENT NEEDED

1. Taco Cycle Test Controller, HP P/N 64932-66501
2. 12-inch IC jumper
3. Oscilloscope

4-12. SERVO TEST PROCEDURE:

a) Remove Tape Controller PCB (see Section II).

b) Remove TACO chip U9 (both the IC and heatsink) and install Servo Test Controller in place of U9.

****
CAUTION
****
Take care not to damage the interconnecting gasket on the Tape Controller PCB.

c) Place Tape Controller PCB on extender board (P/N 64100-66510) and connect I/O Bus ribbon cable (P/N 64100-61605).

d) Connect I/O Bus ribbon cable (HP P/N 64100-61605).

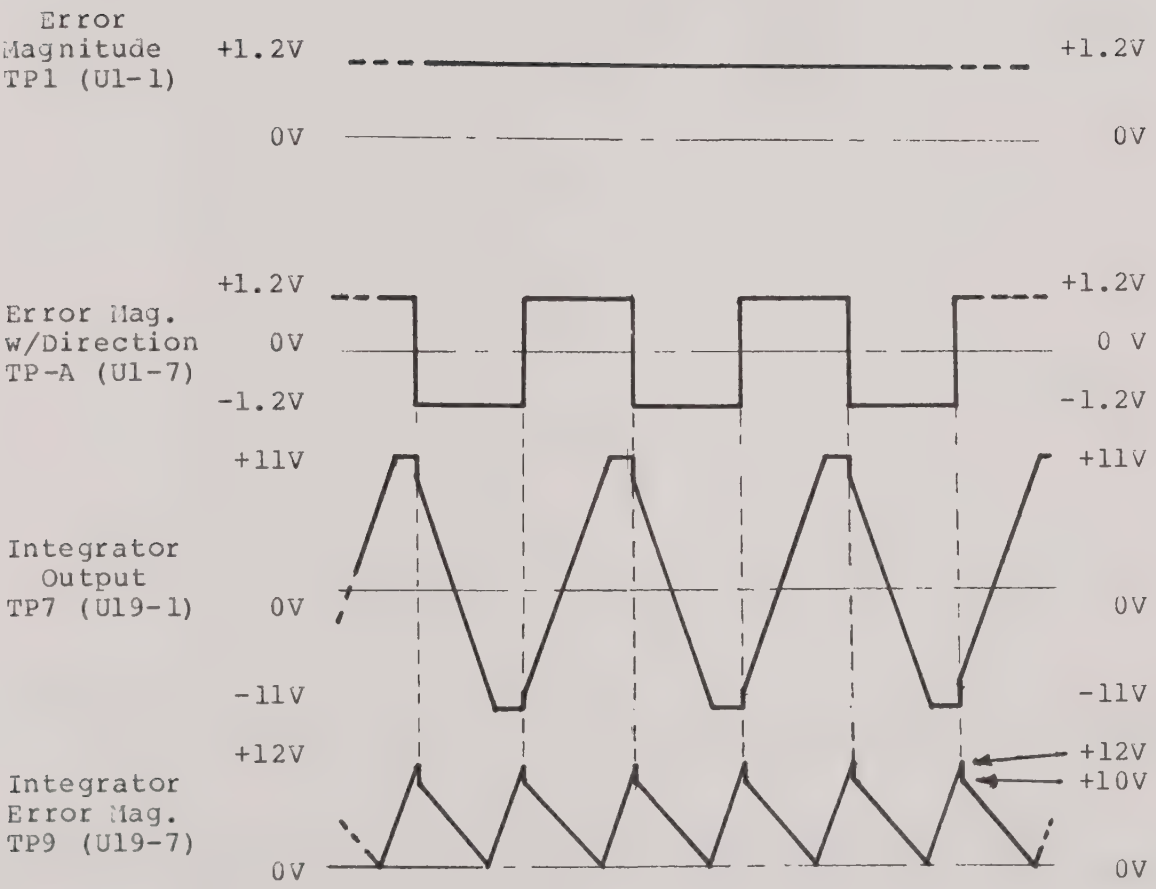
e) Connect the IC jumper between I/O PCB TP2 and Tape Controller PCB U10, pin 9.

f) Power-up system and run PV "Display Test" (this test appears prior to Mainframe PV menu).

g) Connect Transport interconnect cable to check cycling operation of Servo motor.

****
CAUTION
****
This step can be done while the system is under power. However, use caution that the cable polarity is proper and that connection is made slowly with the connector seated squarely on the edge connector.

h) Examine test points for signals shown in Figure 4-1.



NOTE

1. These voltage waveforms are typical from sample PC boards and may vary from system to system.

2. Refer to Tape Controller schematic (sht. 2) for Test Points.

Figure 4-1. SERVO TEST SIGNALS

4-13. SIGNATURE ANALYSIS

4-14. Signature Analysis offers a fast and convenient method of isolating hardware logic failures down to the component level. The basic concept is to utilize a known set of start, stop and clock signals that constantly repeat (loop) with the same timing relationships. When a suspect logic node is probed using these signals together with a Signature Analyzer, the digital readout (signature) displayed on the analyzer can be compared with the normal signature for that node to determine if the timing relationships are proper. With the 64100 Mainframe, looping is provided by the PV software program and the normal signatures for various nodes are listed in Tables 4-2 and 4-3.

NOTE

See the Tape Controller PC board schematics (Figure 8-2) for location Of circuit nodes (i.e., the red letters correspond to the S/A loop being excercised.

4-15. SERVICE TOOLS. Suggested service tools are:

1. HP 5004A Signature Analyzer
2. Digital Voltmeter
3. Oscilloscope
4. Standard hand tools for electronic PC board repair

4-16. Signature Analysis (SA) is available to test the input/output buffers to the Tape Control board. There are two separate tests, the first being more comprehensive than the second.

4-17. The first test assumes that the TACO chip (U9) is working well enough to properly communicate with the I/O Bus. However, if the TACO chip is bad or if the I/O Bus buffers have failed in such a way as to disable the TACO chip functions, then the second SA test should be run.

4-18. PROCEDURE FOR TEST NO. 1:

a) Remove Tape Control board. (See Installation and Removal Section.)

b) Place Tape Control board on extender board (HP Part No. 64100-66510).

c) Connect I/O Bus extender cable (HP Part No. 64100-61605).

d) Connect the Signature Analyzer as follows:

START = I/O board TP2 (rising edge) STOP = I/O board TP2 (falling edge) CLOCK = Tape Control board LIOSB (U10, pin 13) (falling edge).

e) With the Tape Transport cable disconnected, run the tape system PV and verify that V HIGH signature = FF67.

f) Once step (e) is successful, verify LOOP A signatures with reference to the Tape Controller schematics.

4-19. PROCEDURE FOR TEST NO. 2:

a) Remove Tape Control board. (See Installation and Removal Section.)

b) Remove TACO chip U9 from Tape Controller board.

c) Place Tape Controller board on extender board (HP Part No. 64100-66510).

d) Connect I/O Bus extender cable (HP Part No. 64100-61605).

e) Connect Signature Analyzer as follows:

START = I/O board TP2 (rising edge) STOP = I/O board TP2 (falling edge) CLOCK = Tape Control board LIOSB (U10, pin 13) (falling edge).

f) With Tape Transport cable disconnected, run tape system PV and verify that V HIGH signature = FF67.

g) Once step (f) is successful, verify LOOP B signatures with reference to the Tape Controller schematics.

NOTE

Test No.2 tests only the input buffers on the I/O Data Lines. No convenient way exists to test the output buffers. However, a partial test can be done by attaching a jumper between U12, pin 2 and ground. This enables the output buffers. Then by grounding the inputs of these output buffers, you can examine the outputs with a logic probe and verify that they are changing states. Be certain that the states are switching between a logical 1 and a logical 0. See Tape Controller schematic, sht. 1 of 2, for detailed pin assignments (i.e., U2, pin 2 is input; U2, pin 18 is output).

Table 4-2. TAPE CONTROLLER PCB SIGNATURE ANALYSIS (LOOP A)

TEST FAILURE/CKT OR REASON: To test I/O Bus signals to Tape Controller PCB. This test checks control gating and bidirectional data buffers with a working TACO chip (U9) interacting with the I/O Bus.

PROCEDURE: Place tape controller on extender board, and with transport disconnected, run TAPE SYSTEM TEST (PV).

S/A HOOK-UP: START = I/O Board TP2 (rising edge)
STOP = I/O Board TP2 (falling edge)
V = FP67 CLOCK = Tape Controller LIOSB U10-13 (falling edge)
H

NODE	S/A	SIGNAL	NODE	S/A	SIGNAL
U2-2/3	P738	IO0	U7-2/3	FU6P	IO12
18/17	P739	IOD0	18/17	FU6U	IOD12
4/5	HAH8	IO1	4/5	FPU3	IO13
16/15	HAH9	IOD1	16/15	FPU2	IOD13
6/7	F439	IO2	6/7	FP2F	IO14
14/13	F438	IOD2	14/13	FP2H	IOD14
8/9	FC58	IO3	8/9	FP52	IO15
12/11	FC59	IOD3	12/11	FP53	IOD15
			U11-4	FP66	LPA3
U4-2/3	FFU9	IO4	-5	FP67	LPA2
18/17	FFU8	IOD4			
4/5	4U38	IO5	U12-11	0001	LPA1
16/15	4U39	IOD5	-12	0000	LPA0
6/7	8PF9	IO6			
14/13	8PF8	IOD6	U11-3	FP66	LPA0*LPA1
8/9	PP20	IO7	-6	0001	PA3
12/11	PP21	IOD7			
			U10-5	0007	DOUT
			-3	000A	IC2
U5-2/3	HP45	IO8	-1	001U	IC1
18/17	HP44	IOD8			
4/5	F666	IO9	-6	0007	DOUT
16/15	F667	IOD9	-4	000A	IC2
6/7	FA66	IO10	-2	001U	IC1
14/13	FA67	IOD10			
8/9	FF77	IO11			
12/11	FF76	IOD11			

Table 4-3. TAPE CONTROLLER PCB SIGNATURE ANALYSIS (LOOP B)

TEST FAILURE/CKT OR REASON: To test I/O Bus signals going to the TACO chip, U9. This test checks only the input buffers and the control gating.

PROCEDURE: Remove TACO chip, U9. Place Tape Control board on extender board and, with transport disconnected, run Tape System Test (PV).

S/A HOOK-UP: START = I/O Board TP2 (rising edge)
STOP = I/O Board TP2 (falling edge)
V = FP67 CLOCK = Tape Controller LIOSB U10-13 (falling edge)
H

NODE	S/A	SIGNAL	NODE	S/A	SIGNAL
U2-2/3	P73F	IO0	U7-2/3	FU6A	IO12
18/17	P73C	IOD0	18/17	FU6H	IOD12
4/5	HAHF	IO1	4/5	FPU7	IO13
16/15	HAHH	IOD1	16/15	FPU6	IOD13
6/7	F43H	IO2	6/7	FP28	IO14
14/13	F43A	IOD2	14/13	FP2U	IOD14
8/9	FC5F	IO3	8/9	FP56	IO15
12/11	FC5H	IOD3	12/11	FP57	IOD15
U4-2/3	FFUH	IO4	U11-4	FP66	LPA3
18/7	FFUA	IOD4	-5	FP67	LPA2
4/5	4U3F	IO5			
16/15	4U3H	IOD5	U12-11	0001	LPA1
6/7	8PFH	IO6	-12	0000	LPA0
14/13	8PFA	IOD6			
8/9	PP24	IO7	U11-3	FP66	LPA0*LPA1
12/11	PP25	IOD7	-6	0001	PA3
			U10-5	0007	DOUT
U5-2/3	HP41	IO8	-3	000A	IC2
18/17	HP46	IOD8	-1	001U	IC1
4/5	F662	IO9			
16/15	F663	IOD9	U10-6	0007	DOUT
6/7	FA62	IO10	-4	000A	IC2
14/13	FA65	IOD10	-2	001U	IC1
8/9	FF73	IO11			
12/11	FF72	IOD11			

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SECTION V

ADJUSTMENTS AND MAINTENANCE

5-1. GENERAL

5-2. There are no adjustments that can be made to the cartridge tape system. However, there are several maintenance practices which should be followed to extend system reliability.

5-3. TRANSPORT HEAD CLEANING

5-4. The Cartridge Tape Transport may develop a build-up of oxide on the recording heads after several hours of use. The oxide build-up is due to normal operation and may cause errors. Therefore, the read/write head on the Tape Transport should be cleaned approximately every 5 hours of cartridge operation or when a tape problem is suspected. The head cleaning kit contains the necessary materials:

a) Foam swab: HP P/N 9300-0468

b) Magnetic head cleaner: HP P/N 8500-1251

****
CAUTION
****

Cleaning the read/write head with a cotton swab may result in loss of information due to lint from the swab sticking to the tape or head mechanism.

5-5. HEAD CLEANING PROCEDURE:

a) Dip one of the swabs into the bottle of head cleaning solvent to saturate the swab.

b) Hold the transport door open and clean the head with a back-and-forth motion of the swab (not an up-and-down motion).

NOTE

The read/write head is the shiny surface at the right rear of the transport as viewed through the cartridge door.

c) With a dry swab, wipe the head clean with a back-and-forth motion.

5-6. TAPE CARTRIDGE RETHREADING

5-7. Occasionally, it may be necessary to rethread a tape cartridge. Tape rethreading is not recommended unless the data recorded on the runoff tape must be recovered. To perform the following steps you will need these tools:

a) A small phillips-head screwdriver.

b) A long, small-tipped instrument to aid in wrapping the tape around the tape hub.

5-8. RETHREADING PROCEDURE. To rethread the tape cartridge, proceed as follows:

a) Remove the tape cartridge top cover by removing the four screws from the backplate.

NOTE

Whenever the tape cartridge top cover has been removed, be careful the spring-loaded door does not slide off of the pivot post.

b) Rethread the loose end of the tape around the tape guide, through the tape cleaner, past the belt drive puck, outside the guide pin and around the tape guide.

c) Hold the tape cartridge so that the drive belt puck can be rotated while maintaining tape tension.

d) While maintaining tape tension, rotate the belt drive puck to wrap the free end of the tape around the tape hub. Use a long small-tipped instrument to press the tape end into the tape hub until the tape is wrapped several times.

e) Continue wrapping the tape hub until the first set of end-of-tape holes move past the read/write window.

f) Replace the top cover.

g) Condition the tape; i.e., type "tension" then press RETURN

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering parts. Table 6-1 lists the names and addresses that correspond to the manufacturers' code numbers. Table 6-2 lists the abbreviations used in the parts list and throughout this manual. Table 6-3 lists all replaceable parts for the Tape Controller PC board in reference designator order.

6-3. ABBREVIATIONS

6-4. Table 6-2 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases two forms of the abbreviation are used; one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

6-5. ILLUSTRATED PARTS BREAKDOWN

6-6. Figure 6-1 is the Illustrated Parts Breakdown for removable (unsoldered) parts of the Tape Controller PC board. This figure illustrates the assembly/dissasembly order and the identity of the mounting hardware. To find the location and identity of the electrical components, refer to the component locator diagram (Figure 8-1) in Section VIII.

6-7. MAJOR COMPONENTS

6-8. The following major components comprise the Model 64940A Tape System:

1. Tape Controller PC board ..... HP P/N 64940-66501
2. Tape Transport Assy ..... HP P/N 98075A
3. Ribbon Cable, 2-Connector..... HP P/N 64940-61601
4. Ribbon Cable, 3-Connector..... HP P/N 64940-61602
5. Front Panel ..... HP P/N 5041-1532
6. Mini-cassette Tape ..... HP P/N 5061-3660

Table 6-1. LIST OF MANUFACTURERS' CODES

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier	------	------
00466	Norelco N. Amer philips Corp	Los Angeles Ca	90021
01121	Allen-Bradley Co	Milwaukee Wi	53204
01295	Texas Instr Semicond Div	Dallas Tx	75222
01928	RCA Corp Solid State Div	Somerville NJ	08876
03888	KDI Pyrofilm Corp	Whippany NJ	07981
04713	Motorola Semicond Products	Phoenix Az	85062
07263	Fairchild Semicond Div	Mountain View Ca	94042
09023	Cornell-Dubilier Eleck Div	Sanford NC	27330
13103	Thermalloy Co	Dallas Tx	75234
19701	Mepco/Electra Corp	Mineral Wells Tx	76067
20940	Micro-Ohm Corp	El Monte Ca	91731
24546	Corning Glass Wks	Bradford Pa	16701
26654	Varadyne Inc	Santa Monica Ca	90404
27014	National Semicond Corp	Santa Clara Ca	95051
27777	Varo Semicond Inc	Garland Tx	75040
28480	Hewlett-Packard Hq	Palo Alto Ca	94304
30983	Mepco/Electra Corp	San Diego Ca	92121
32997	Bourns Trimpot Div	Riverside Ca	92507
34344	Motorola Inc	Franklin Park Il	60131
34649	Intel Corp	Mountain View Ca	95051
56289	Sprague Elect Co	North Adams Ma	01247
71590	Centralab Eleck Div	Milwaukee Wi	50501
72136	Electro Motive Corp	Willimantic Ct	06226
75042	TRW Inc	Philadelphia Pa	19108
75382	Kulka Elect Corp	Mt Vernon NY	10550
75915	Littlefuse Inc	Des Plaines Il	60016

6-9. ORDERING INFORMATION

6-10. To order a part listed in the replaceable parts list (Table 6-3), quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Office (refer to Sales and Service offices listed at the back of this manual).

6-11. To order a part that is not listed in Table 6-3, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-12. DIRECT MAIL ORDER SYSTEM

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

1. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

2. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

3. Prepaid transportation (there is a small handling charge for each order).

4. No invoices (to provide these advantages, a check or money order must accompany each order).

6-14. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

6-15. PARTS LIST

6-16. Table 6-3 lists the replaceable parts for the Tape Controller PCB and is organized as follows:

1. Electrical assemblies and their components in alphanumerical order by reference designation.

2. Miscellaneous parts.

6-17. The information given for each part consists of the following:

1. Hewlett-Packard part number and check digit. (for HP internal use).

2. Total quantity (Qty) on the PC board.

3. Description of the part.

4. Typical manufacturer of the part in a five-digit code.

5. Manufacturer's number for the part.

NOTE

The total quantity for each part is given only at the first appearance of the part number in the list.

Table 6-2. Abbreviations

REFERENCE DESIGNATORS

A	= assembly	F	= fuse	MP	= mechanical part	U	= integrated circuit
B	= motor	FL	= filter	P	= plug	V	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	IC	= integrated circuit	Q	= transistor		
C	= capacitor	J	= jack	R	= resistor	VR	= voltage regulator
CP	= coupler	K	= relay	RT	= thermistor	W	= cable
CR	= diode	L	= inductor	S	= switch	X	= socket
DL	= delay line	LS	= loud speaker	T	= transformer	Y	= crystal
DS	= device signaling (lamp)	M	= meter	TB	= terminal board	Z	= tuned cavity network
E	= misc electronic part	MK	= microphone	TP	= test point		

ABBREVIATIONS

A	= amperes	H	= henries	N/O	= normally open	RMO	= rack mount only
AFC	= automatic frequency control	HDW	= hardware	NOM	= nominal	RMS	= root-mean square
AMPL	= amplifier	HEX	= hexagonal	NPO	= negative positive zero (zero temperature coefficient)	RWV	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	HR	= hour(s)				
BE CU	= beryllium copper	HZ	= hertz	NPN	= negative-positive-negative	S-B	= slow-blow
BH	= binder head					SCR	= screw
BP	= bandpass			NRFR	= not recommended for field replacement	SE	= selenium
BRS	= brass	IF	= intermediate freq			SECT	= section(s)
BWO	= backward wave oscillator	IMPG	= impregnated	NSR	= not separately replaceable	SEMICON	= semiconductor
		INCD	= incandescent			SI	= silicon
CCW	= counter-clockwise	INCL	= include(s)			SIL	= silver
CER	= ceramic	INS	= insulation(ed)	OBD	= order by description	SL	= slide
CMO	= cabinet mount only	INT	= internal	OH	= oval head	SPG	= spring
COEF	= coeficient			OX	= oxide	SPL	= special
COM	= common	K	= kilo=1000			SST	= stainless steel
COMP	= composition					SR	= split ring
COMPL	= complete	LH	= left hand	P	= peak	STL	= steel
CONN	= connector	LIN	= linear taper	PC	= printed circuit		
CP	= cadmium plate	LK WASH	= lock washer	PF	= picofarads= 10^{-12} farads	TA	= tantalum
CRT	= cathode-ray tube	LOG	= logarithmic taper			TD	= time delay
CW	= clockwise	LPF	= low pass filter	PH BRZ	= phosphor bronze	TGL	= toggle
				PHL	= phillips	THD	= thread
DEPC	= deposited carbon	M	= milli=10^{-3}	PIV	= peak inverse voltage	TI	= titanium
DR	= drive	MEG	= meg=10^{6}	PNP	= positive-negative-positive	TOL	= tolerance
		MET FLM	= metal film			TRIM	= trimmer
ELECT	= electrolytic	MET OX	= metallic oxide	P/O	= part of	TWT	= traveling wave tube
ENCAP	= encapsulated	MFR	= manufacturer	POLY	= polystyrene		
EXT	= external	MHZ	= mega hertz	PORC	= porcelain	U	= micro=10^{-6}
		MINAT	= miniature	POS	= position(s)		
F	= farads	MOM	= momentary	POT	= potentiometer	VAR	= variable
FH	= flat head	MOS	= metal oxide substrate	PP	= peak-to-peak	VDCW	= dc working volts
FIL H	= fillister head	MTG	= mounting	PT	= point		
FXD	= fixed	MY	= "mylar"	PWV	= peak working voltage	W/	= with
						W	= watts
G	= giga (10^{9})	N	= nano (10^{-9})	RECT	= rectifier	WIV	= working inverse voltage
GE	= germanium	N/C	= normally closed	RF	= radio frequency		
GL	= glass	NE	= neon	RH	= round head or right hand	WW	= wirewound
GRD	= ground(ed)	NI PL	= nickel plate			W/O	= without

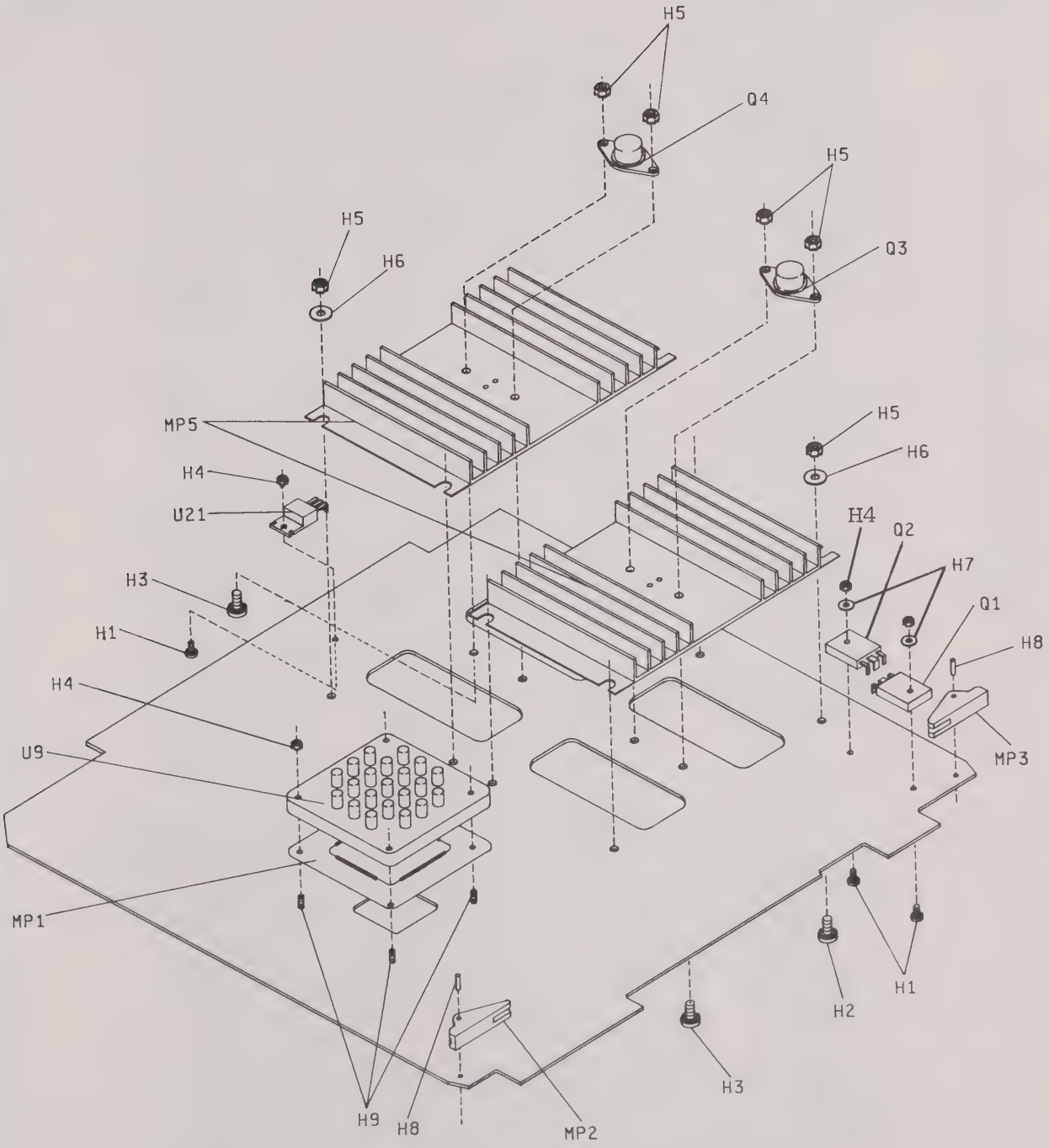

Figure 6-1. Controller PCB Illustrated Parts Breakdown

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64940-66501	1	1	TAPE CONTROLLER (TACO) PC BOARD	28480	64940-66501
C1	0160-3619	3	1	CAPACITOR-FXD 680PF +-10% 100VDC CER	28480	0160-3619
C2	0160-2055	9	15	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C3	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C6	0160-0127	2	1	CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C9	0160-2197	0	1	CAPACITOR-FXD 10PF +-5% 300VDC MICA	28480	0160-2197
C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C12	0140-0190	7	1	CAPACITOR-FXD 39PF +-5% 300VDC MICA	72136	DM15E390J0300WV1CR
C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C15	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C16	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C17				NOT USED		
C18				NOT USED		
C19				NOT USED		
C20	0180-1819	3	1	CAPACITOR-FXD 100UF+75-10% 50VDC AL	56289	30D107G050DM2
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C22				NOT USED		
C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C27	0180-1745	4	4	CAPACITOR-FXD 1.5UF+-10% 20VDC TA	56289	150D155X9020A2
C28	0180-1745	4		CAPACITOR-FXD 1.5UF+-10% 20VDC TA	56289	150D155X9020A2
C29	0180-1745	4		CAPACITOR-FXD 1.5UF+-10% 20VDC TA	56289	150D155X9020A2
C30	0180-1745	4		CAPACITOR-FXD 1.5UF+-10% 20VDC TA	56289	150D155X9020A2
C31	0180-1784	1	1	CAPACITOR-FXD 1000UF+75-10% 40VDC AL	28480	0180-1784
C32	0160-3638	6	1	CAPACITOR-FXD .22UF +80-20% 200VDC CER	28480	0160-3638
C33	0160-3622	8	1	CAPACITOR-FXD .1UF +80-20% 100VDC CER	28654	2130Y5V100R104Z
C34	0160-3448	6	2	CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3448
C35	0160-3448	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3448
C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C37	0180-0104	7	1	CAPACITOR-FXD 200UF+75-10% 16VDC AL	56289	30D207G016DF2
CR1	1901-0028	5	2	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
CR2	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
CR3	1901-0040	1	3	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR6	1910-0016	0	1	DIODE-GE 60V 60MA 1US DO-7	28480	1910-0016
F1	2110-0002	9	1	FUSE 2A 250V FAST-BLO 1.25X.25 UL	75915	312002
H1	2200-0105	8	1	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H2	2360-0117	6	8	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H3	2360-0121	2	4	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H4	2260-0009	3	7	NUT-HEX-W/LKWR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H5	2420-0001	5	12	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
H6	3050-0066	8	8	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
H7	3050-0425	3	2	WASHER-FL MTLC .125-IN-ID .312-IN-OD SST	28480	3050-0425
H8	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
H9	0360-0679	3	4	TERMINAL-STUD SPCL-STDF PRESS-MTG	28480	0360-0679
L1-L2	9140-0210	1	2	COIL-MLD 100UH 5% Q=50 .155DX.375LG-NOM	28480	9140-0210
L3	9140-0171			COIL-MLD 40UH 5% Q=50	28480	9140-0171
MP1	09845-67904	8	1	CONDUCTIVE GASKET 488Y (FOR TACO CHIP U9)	28480	09845-67904
MP2	0403-0368	9	1	EXTRACTOR, PC BOARD ("TAPE")	28480	0403-0368
MP3	0403-0369	0	1	EXTRACTOR, PC BOARD ("64940A")	28480	0403-0369
MP4	2110-0269	0	1	FUSEHOLDER-CLIP TYPE,25D-FUSE	28480	2110-0269
MP5	1205-0380	6	2	HEAT SINK SPCL-HOLE-PATT	28480	1205-0380
Q1	1854-0558	5	2	TRANSISTOR NPN SI DARL PD=70W FT=1MHZ	28480	1854-0558
Q2	1854-0558	5		TRANSISTOR NPN SI DARL PD=70W FT=1MHZ	28480	1854-0558
Q3	1853-0383	2	2	TRANSISTOR PNP 2N6296 SI DARL TO-66	04713	2N6296
Q4	1853-0383	2		TRANSISTOR PNP 2N6296 SI DARL TO-66	04713	2N6296
Q5	1854-0215	1	2	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
Q6	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
Q7	1855-0082	2	2	TRANSISTOR J-FET P-CHAN D-MODE SI	28480	1855-0082
Q8	1855-0082	2		TRANSISTOR J-FET P-CHAN D-MODE SI	28480	1855-0082
TP1(	1251-2229	0	1	TEST POINT PIN SOCKET	00000	ORDER BY DESCRIPTION
** GND SHLD	1251-4045	0	1	TEST POINT GND SHIELD	00000	ORDER BY DESCRIPTION

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R1	0684-5611	9	5	RESISTOR 560 10% .25W FC TC=-400/+600	01121	CB5611
R2	0757-0288	1	3	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
R3	0757-0431	6	4	RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
R4	0684-1041	1	3	RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
R5	0684-6821	5	2	RESISTOR 6.8K 10% .25W FC TC=-400/+700	01121	CB6821
R6	0757-0431	6		RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
R7	0757-0288	1		RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
R8	0684-1041	1		RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
R9	0757-0288	1		RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
R10	0757-0424	7	1	RESISTOR 1.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1101-F
R11	0684-6821	5		RESISTOR 6.8K 10% .25W FC TC=-400/+700	01121	CB6821
R12	0684-3321	4	2	RESISTOR 3.3K 10% .25W FC TC=-400/+700	01121	CB3321
R13	0811-1553	1	3	RESISTOR .68 5% 2W PW TC=0+-800	75042	BWH2-11/16-J
R14	0757-0414	5	4	RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
R15	0757-0414	5		RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
R16	0684-8211	1	2	RESISTOR 820 10% .25W FC TC=-400/+600	01121	CB8211
R17	0684-8211	1		RESISTOR 820 10% .25W FC TC=-400/+600	01121	CB8211
R18	0684-5611	9		RESISTOR 560 10% .25W FC TC=-400/+600	01121	CB5611
R19	0684-5611	9		RESISTOR 560 10% .25W FC TC=-400/+600	01121	CB5611
R20	0684-5611	9		RESISTOR 560 10% .25W FC TC=-400/+600	01121	CB5611
R21	0684-5611	9		RESISTOR 560 10% .25W FC TC=-400/+600	01121	CB5611
R22	0684-3341	8	2	RESISTOR 330K 10% .25W FC TC=-800/+900	01121	CB3341
R23	0757-0414	5		RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
R24	0684-3321	4		RESISTOR 3.3K 10% .25W FC TC=-400/+700	01121	CB3321
R25	0757-0283	6	4	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R26	0757-0451	0	1	RESISTOR 24.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2432-F
R27	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R28	0684-1031	9	2	RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
R29	0684-1021	7	6	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R30	0684-1041	1		RESISTOR 100K 10% .25W FC TC=-400/+800	01121	CB1041
R31	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R32	0684-1031	9		RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
R33	0757-0453	2	3	RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
R34	0757-0453	2		RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
R35	0757-0453	2		RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
R36	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R37	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R38	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R39	0757-0281	4	1	RESISTOR 2.74K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2741-F
R40	0684-2721	6	1	RESISTOR 2.7K 10% .25W FC TC=-400/+700	01121	CB2721
R41	0757-0431	6		RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
R42	0757-0431	6		RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
R43	0684-3311	2	2	RESISTOR 330 10% .25W FC TC=-400/+600	01121	CB3311
R44	0684-3341	8		RESISTOR 330K 10% .25W FC TC=-800/+900	01121	CB3341
R45	0684-2221	1	6	RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
R46	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
R47	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
R48	0683-1825	7	2	RESISTOR 1.8K 5% .25W FC TC=-400/+700	01121	CB1825
R49	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R50	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R51	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R52	0683-1825	7		RESISTOR 1.8K 5% .25W FC TC=-400/+700	01121	CB1825
R53	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R54	0757-0414	5		RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
R55	0684-6831	7	1	RESISTOR 68K 10% .25W FC TC=-400/+800	01121	CB6831
R56	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
R57	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
R58	0684-3311	2		RESISTOR 330 10% .25W FC TC=-400/+600	01121	CB3311
R59	0684-2221	1		RESISTOR 2.2K 10% .25W FC TC=-400/+700	01121	CB2221
R60	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
R61				NOT USED		
R62				NOT USED		
R63				NOT USED		
R64				NOT USED		
R65				NOT USED		
R70	0811-1553	1		RESISTOR .68 5% 2W PW TC=0+-800	75042	BWH2-11/16-J
R71	0811-1553	1		RESISTOR .68 5% 2W PW TC=0+-800	75042	BWH2-11/16-J
TP1-TP9 plus GNDs	0360-1971	0	11	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1826-0139	9	1	IC OP AMP GP DUAL 8-DIP-P	01928	CA1458G
U2	1820-1918	2	4	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
U3	1810-0277	3	3	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
U4	1820-1918	2		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
U5	1820-1918	2		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U6	1810-0277	3		NETWORK-RES 10-8IP2.2K OHM X 9	01121	210A222
U7	1820-1918	2		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
U8	1826-0188	8	1	IC CONV 8-B-D/A 16-DIP-C	04713	MC1408L-8
U9	5061-3012	5	1	HYBRID TACO CHIP (TAPE CONTROLLER)	28480	5061-3012
U10	1820-0668	7	1	IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
U11	1820-1414	3	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS12N
U12	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U13	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U14	1820-1282	3	1	IC FF TTL LS J-K BAR POS-EDGE-TRIG	01295	SN74LS109AN
U15	1820-0981	7	1	IC SWITCH ANLG QUAD 14-DIP-P	01928	CD4016AE
U16	1810-0280	8	1	NETWORK-RES 10-8IP10.0K OHM X 9	01121	210A103
U17	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
U18	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P	04713	MLM339P
U19				IC, OP AMP MC1458		
U20	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P	01295	SN72311P
U21	1826-0478	9	1	IC 7906 V REGLTR TO-220	07263	UA7906UC
U22	1810-0277	3		NETWORK-RES 10-8IP2.2K OHM X 9	01121	210A222
VR1	1902-3036	3	2	DIODE-ZNR 3.16V 5% DO-7 PD=.4W TC=-.064%	28480	1902-3036
VR2	1902-3036	3		DIODE-ZNR 3.16V 5% DO-7 PD=.4W TC=-.064%	28480	1902-3036
VR3	1902-0041	4	1	DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=-.009%	28480	1902-0041
VR4	1902-3203	6	1	DIODE-ZNR 14.7V 5% DO-7 PD=.4W TC=+.057%	28480	1902-3203

SECTION VII

BACKDATING

7-1. INTRODUCTION

7-2. This section contains information for adapting this manual to Tape Controller and Drive units with earlier repair prefix numbers.

7-3. MANUAL CHANGES

7-4. To adapt this manual to your cassette tape system, make the manual changes listed in Table 7-1 under the repair prefix number for your system. Perform these changes in the order listed.

Table 7-1. REPAIR NO. vs. MANUAL CHANGE NO.

REPAIR PREFIX	MAKE CHANGES

NOTE

There is no Backdating information for the Cassette Tape System at the publication date this manual.

7-5. MANUAL CHANGE INSTRUCTIONS

NOTE

There are no manual changes applicable at the publication date of this manual.

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SECTION VIII

THEORY AND SCHEMATICS

8-1. INTRODUCTION

8-2. This Section contains the theory-of-operation for the Cassette Tape System. The first part discusses the Block Diagram functions while the second part elaborates on these functions by referring to detailed circuit schematics and appropriate truth tables.

8-3. BLOCK DIAGRAM DESCRIPTION (FIGURE 8-2)

8-4. The Cassette Tape System consists of four major functional areas: 1) Control Section, 2) Servo Section, 3) Read/Write Electronics, and 4) the Tape Transport. These four functional areas are discussed to the block diagram level in the following paragraphs.

8-5. CONTROL SECTION (BLOCK DIA. DESCRIP.)

8-6. The Control Section is the heart of the cassette tape system in that it performs all of the control functions required for storing and retrieving data from magnetic tape. The Control Section also provides the interface through which the 64100 Mainframe CPU communicates with the tape system. This communication consists of: 1) the CPU telling the Tape System when to write and read data from the magnetic tape, and 2) the necessary "handshaking" that coordinates the transfer of data and instructions between the CPU and the tape system. The major functions of the Control Section are listed in Table 8-1.

Table 8-1. CONTROL SECTION FUNCTIONS

1. Interfaces with external CPU (i.e., "handshaking", control, and data transfer).
2. Controls record and playback of 16-bit data word using a delta-distance encoding technique.
3. Controls two-way flow (double buffering) of data/instruction words per software instructuons.
4. Pre-compensates bit lengths when writing to eliminate interference with adjacent bits.
5. Interrupts the CPU when an instruction is completed or data is needed.
6. Measures distance on tape, measuring gaps and detects "end-of-valid data" marks.

7. Reads and writes in HP Standard Interchange Format (SIF) per software instructions.

8. Calculates checksum to detect bit errors during read and write.

9. Controls tape speed and direction per software instructions.

8-7. The Control Section consists of five major circuits: 1) Tape Control Chip U9 (TACO), 2) Logic Gates and Buffers U10, U11 and U12, 3) Transceivers U2, U4, U5, and U7, 4) 4-1Hz Oscillator U13, and 5) Initiate Logic U13, U14, and U17 (see Figure 8-2).

8-8. TAPE CONTROL IC CHIP. The TACO chip is a self-contained microprocessor that is specifically designed for controlling the cassette tape system. The nine major functions provided by the TACO chip are listed in Table 8-1 above.

8-9. There are eight major signal groups that comprise the input/output of U9 (see Figure 8-2). The function of these signal groups are summarized in Table 8-2.

Table 8-2. TACO CHIP I/O SIGNAL GROUPS

SIGNAL GROUP	FUNCTION
A. I/O Data	16 data lines that are used for two-way communication with the TACO chip.
B. External TACO Control	These signals originate in the external CPU. They control: U9 select, interrupt polling, latching data into U9, direction of I/O data flow, and U9 internal register select.
C. Internal TACO Control	These signals originate within the cassette tape system. They provide the following functions: U9 initialization, U9 clock input, write protect status, tape hole status, and cartridge in/out status.
D. Read/Write Control	These signals control the read/write mode and which track (A or B) is being used.

E. Read Data	These two signals comprise the read (playback) data. The flux reversal signal (FR) represents data when tape speed is less than 22 ips. Threshold signal (THR) represents data for tape speeds greater than 22 ips.
F. Write Data	This signal comprises the data that is to be written on mag tape.
G. Servo Control and Status	These signals control tape speed and monitor the status of the servo circuit.
H. TACO Status	This group includes the TACO interrupt request signal and two status signals. The interrupt request signal tells the CPU that the TACO has data ready for it. The status signals tell the CPU that TACO is ready to accept data from the CPU and that no error conditions exist.

8-10. LOGIC GATES, BUFFERS, AND XCVRS. The external control signals pass through a series of buffers before being applied to the TACO chip. The I/O data passes through four bi-directional data transceivers that are enabled and disabled by bus drive signal BD from the TACO chip.

8-11. OSCILLATOR and INITIATE LOGIC. Timing for the TACO chip is provided by a 4-MHz Oscillator circuit. The Initiate Logic uses the power-on pulse (LPOP) from the 64100 Mainframe and the 4-MHZ clock as inputs and ensures that both of these signals are present before generating the initiate signal INIT. This circuit also assures that sufficient time has passed for the clock and power circuits to stabilize after turn-on. This delay prevents accidental writing of data on the tape during power-on.

8-12. READ/WRITE CIRCUITS

8-13. TACH PULSE and TAPE HOLE DETECTORS. The analog tach control (ATC) and tape hole (HOL) output signals from the tach wheel and tape hole phototransistors (on the Tape Transport) are fed to the Tach Pulse Detector and the Hole Detector Amp, respectively. These two circuits detect and amplify the respective signals while providing noise immunity by introducing a small amount of hysteresis to the two signals.

8-14. The HOL signals are used to indicate the "load-point" and "end-of-tape" positions on the mag tape. The ATC signal is used by U9 to regulate tape speed for consistant reading and writing of data.

8-15. WRITE CURRENT and READ/WRITE CONTROL. Write data (WDT) from the TACO chip is applied to the Read/Write Control circuit where it modulates the record-head current. Write signal (WRT) controls the read/write mode and is applied to both the Read/Write Control and the Write Current Source circuits. When WRT is high, the write current source circuit is enabled and write current is provided for the Read/write head. When WRT is low, the write current is disabled and the read circuits can then reproduce the recorded signal. The Track B select signal (TRB) is also applied to the Read/Write Control circuit where it selects either track A or track B for writing. The initiate signal (INIT) momentarily disables the write current circuit while the clock and power supply signals are stabilizing after the system is turned on.

8-16. READ/WRITE HEAD. The Read/Write head stores binary information on the magnetic tape by causing flux reversals to occur corresponding to the logic state of the data string being recorded. A binary one is distinguished from a binary zero by a delta-distance coding scheme in which the one bit is 1.75 times longer than the zero bit.

8-17. Two head-windings are utilized for recording two tracks, A and B. Each head-winding is also a split configuration in which one half is used for recording positive-going transitions and the other half for negative going transitions. Thus, during writing only one half of the head is used at a time. During read, both halves of the head are sensed in order to detect both types of flux reversals.

8-18. PREAMP and LOWPASS FILTER. The Preamp provides about 20 db gain to the playback signal. There are adjustments provided that are used for balancing the playback signal from each track and both segments of each headwinding. The Lowpass Filter is an active filter that provides some gain while eliminating any high frequency noise that might be present in the playback signal.

8-19. DIFFERENTIATOR, THRESHOLD and ZERO-CROSSING DETECTORS. The Differentiator differentiates the playback signal to determine the peak level of the signal. The Threshold Detector detects when the playback signal exceeds a pre-set voltage threshold determined by the TACO chip and communicated to the threshold circuit via the mode (MOD) signal.

8-20. The Zero-Crossing Detector senses when flux reversals occur (by detecting zero crossings) and produces an alternately positive or negative signal at each reversal. The Zero-Crossing Detector is inhibited until the threshold circuit has determined that the minimum threshold has been exceeded (i.e., THR must be present before FR can be produced). Both the flux reversal signal (FR) and threshold signal (THR) are sent to the TACO chip where they are used for detecting gaps and timing the length of the data bits. FR represents read data when the tape speed is 22 ips or less; THR represents read data when the tape speed is greater than 22 ips.

8-21. TAPE TRANSPORT ASSEMBLY (BLOCK DIA. DESCRIP.)

8-22. The Tape Transport houses the mechanical components of the cassette tape system. The Tape Transport components involved in the control of the tape system include:

1. Tape Moving Indicator
2. Tachometer Wheel and Sensor
3. Tape Hole Sensor
4. Cartridge-in Switch
5. Write Protect Switch

8-23. TAPE INDICATOR. The Tape Moving Indicator is a LED located on the front panel to the left of the cartridge slot and is driven by the tape drive-on signal (TDRON) from the TACO chip. The TDRON signal is present (high) anytime tape speed is greater than 2 ips and consequently lights the LED. When tape speed falls below 2 ips, the LED is extinquished.

8-24. TACH PULSE. Tape speed is sensed by use of a slotted tachometer wheel, an incandescent light source, and a phototransistor light detector. The tach wheel has 968 slots that correspond to one inch of tape movement. The tach wheel is attached to one end of the drive motor shaft and thus rotates anytime the tape is being driven. The light source is located on one side of the tach wheel and the phototransisitor on the opposite side such that the phototransistor can detect the light pulses as the tach wheel rotates. These light pulses produce the analog tach control signal ATC.

8-25. TAPE HOLE SENSOR. The magnetic recording tape uses a series of holes at either end to indentify the beginning and end of the useable recording area. These holes are detected in a manner similar to the tach pulses. In this case, the light source is located underneath the tape transport cassette slot. The light passes through a small pin-hole underneath the cassette cartridge. This pin-hole is located such

that the light beam is reflected by a 45-degree mirror located in the cartridge. The light beam then passes through the tape path and (if a hole is present) on out the back of the cartridge and impinges on a phototransistor located at the rear of the cartridge slot. The output of the phototransistor is detected and amplified to produce the tape hole signal (HOL) which is fed to the TACO chip.

8-26. CARTRIDGE and WRITE PROTECT SWITCHES. There are two switch buttons located at the left-rear of the cartridge slot. The lower switch button is the Cartridge Switch and is closed by inserting the cassette cartridge. This produces the cartridge-in signal (CIN) which informs the TACO chip that the cartridge is inserted.

8-27. The upper switch button is the Write Protect switch. The operator has the option of controlling the state of this switch by positioning the RECORD slide tab on the cassette cartridge in either the record position or the non-record position. When in the latter position, this switch creates the write protect signal (WRP) which disables the write circuits and also informs the TACO chip of the status.

8-28. SERVO SECTION (BLOCK DIA. DESCRIP.)

8-29. TACH SIGNAL and ERROR SIGNAL. The analog tach control (ATC) pulses from the Tach Pulse Detector are fed to the Pulse Shaper circuit where they are converted into a squarewave signal called frequency feedback (FF). This signal is sent to the TACO chip where it is used for computing the speed error.

8-30. The speed error is represented by two outputs from the TACO chip: 1) the speed error magnitude (i.e., how fast or slow) is represented by digital signals DA0 through DA4, and 2) the direction in which the correction has to be made (i.e., accelerate in the forward or reverse direction) is represented by the SIGN signal. These two signal types are sent to the Servo Section where they are ultimately used for correcting the tape speed.

8-31. D/A CONVERTER and CURRENT-TO-VOLTAGE CONVERTER. The 5-bit error signal (DA0 thru DA4) is converted into an analog current that represents the instantaneous error magnitude. This signal is then fed to a current-to-voltage converter where it is converted into a voltage signal.

8-32. BUFFER and DIRECTION GATING. The SIGN signal is first buffered and then to sent the Direction Gating circuit. This circuit produces two control signals: FWD (forward) and REV (reverse). The FWD signal causes the tape speed to accelerate in the foward direction. The REV signal causes the tape to accelerate in the reverse direction.

8-33. ACCEL/DECEL DISCRIMINATOR and INTEGRATOR. The error signal and direction gating signals are summed by the Accel/Decel Discriminator circuit. This produces a composite signal that controls both the direction in which the tape is accelerated and the instantaneous rate of change. The output of this circuit is negative if the tape speed is to be accelerated in the forward direction and positive if the converse is true.

8-34. INTEGRATOR. This circuit acts like a filter in that it smooths (averages) the instantaneous perturbations in the error signal. This reduces the stress on the tape and drive components due to attempting to change tape speed and direction almost instantaneously when near the target speed crossover point (either 22 or 90 ips).

8-35. The integrated error signal consists of two components: a) the absolute voltage magnitude which determines the acceleration rate, and b) the voltage polarity which determines the direction the tape is to be accelerated. The acceleration rate can vary between zero and a maximum of 1200 ips which corresponds to the voltage range of zero to plus or minus 12 volts. When the error voltage is positive, the tape is accelerated in the positive direction; when negative the converse is true.

8-36. ERROR MAGNITUDE, DIRECTION COMPARATOR, and CLAMP CKTS. The Error Magnitude circuit ignores the polarity of the integrated error signal and produces a positive-polarity signal representing only the absolute value of the error signal. The output of this circuit passes through the Clamp and Drive Switch circuits and thence to the Forward Drive circuits where it controls the amount of drive current that is applied to the drive motor.

8-37. The Direction Comparator ignores the absolute value of the integrated error signal and produces two control signals: Forward and Reverse. These signals control the on/off state of the Forward and Reverse Switches.

8-38. The Clamp circuit is a FET switch that is conrolled by the tape drive-on signal (TDRON). This signal turns on the Clamp switch when the TACO chip has determined that the tape speed has dropped lower than 2 ips. Turning the Clamp switch on grounds the error signal thus preventing the drive motor from creeping.

8-39. DRIVE SWITCHES, DRIVE SOURCES/SINKS and DRIVE MOTOR. The forward and reverse drive switches pass the error magnitude signal on to either the forward or reverse drive current sources. The drive switches are controlled by the Direction Comparator output signal.

8-40. The forward and reverse drive source circuits provide the drive current for the tape drive motor. Conversely, the forward and reverse drive sink circuits provide a current path to ground for the drive currents. The drive motor is a compact dc motor capable of driving in either direction.

8-41. SERVO-FAIL DETECTOR. This circuit provides drive motor overload protection by sensing the amount of drive current passing through the motor. When the drive current reaches a preset threshold, this circuit produces the SFAIL signal which informs the TACO chip that a failure condition exists.

8-42. SCHEMATIC DESCRIPTION (Figure 8-3, shts. 1 and 2)

8-43. This section provides additional detailed information concerning the Control and Servo circuits. The Tape Transport assembly and Read/Write circuits are not covered at this level since they are replaced as a unit in case of failure.

8-45. LOGIC CONVENTION. The positive logic convention is used for logic variables and circuits comprising the 64940A cassette system. This convention defines a logic 1 as the more positive voltage (high) and a logic 0 as the more negative voltage (low). All integrated circuit logic devices in the 64940A are 7400 devices and ultilize transistor-to-transistor logic (TTL) levels. Ideally, the low and high voltage levels for 7400 devices are 0V and +5V, respectively. But due to voltage drops over the interconnecting PC board traces and other causes, the actual levels can vary from these ideal values. Therefore, the voltage levels for a logic 1 and 0 are defined as follows:

TTL VOLTAGE LEVELS

QUANTITY		VOLTAGE LIMIT
Input	0	< 0.8V
Input	1	> 2.0V
Output	0	< 0.4V
Output	1	> 2.4V

8-45. MNEMONICS. Signals in the 64940A have been assigned mnemonics that describe the active state and function of the signal line (see Table 8-3). A prefix letter (H or L) or superscript bar is used to indicate the active state of the signal and the remaining letters indicate its function. A "H" prefix or the absence of a bar indicates that the function is active in the "high" state; a "L" prefix or the presence of a bar above a mnemonic indicates that the function is active in the low state.

8-46. SIGNATURE ANALYSIS LOOPS. The red letters on the 64940A schematics indicate circuit nodes where signature analysis "signatures" have been taken to aid in troubleshooting the logic circuits. Refer to Section IV for instructions on how to use signature analysis for troubleshooting. Figure 8-1 identifies the componenets on the Tape Controller PC board.

8-47. TAPE CONTROLLER IC U9. The nine basic functions of the Tape Controller (TACO) IC chip were summarized earlier in Table 8-1 and the eight major signal groups were defined in Table 8-2. How these functions are implememted by the TACO chip is briefly described in the following paragraphs.

8-48. The TACO chip is controlled by system software instructions residing in the TACO driver programs. These instructions are processed by the external CPU and communicated to the TACO chip via the I/O Data and Control Bus. Most of these instructions, together with the read/write data, arrive over the 16 I/O data lines (IOD0-IOD15). These instructions include the four tape motion commands (fast, slow, forward, and reverse) plus a series of commands that select various read/write modes (track select, stop tape, move tape, interrupt, write format, read checksum, etc.). The remaining instructions and control signals (External TACO Control) also arrive from the CPU over the I/O bus but are concerned mainly with "handshake" functions, TACO chip select, and TACO internal register select. The only signals arriving via the Motherboard bus are the power inputs and power-on pulse LPOP. The LPOP signal clocks flip-flops U14A and U14B to generate initiate signal INIT.

8-49. The TACO chip is selected by peripheral addresses LPA0-LPA3 according to the following truth table:

U9 CHIP SELECT TRUTH TABLE

LPA3	LPA2	LPA1	LPA0	TACO Selected
1	1	0	0	Yes
All other conditions				No

8-50. The TACO stores instructions, data and status words in seven internal storage registers:

1. HOLDING REGISTER. Acts as interim storage for I/O data word; data word is transferred to appropriate internal register as determined by interface commands IC1 and IC2:

U9 REGISTER SELECT TRUTH TABLE

DOUT	IC2	IC1	Selected Register
X	0	0	Data Reg.
X	0	1	Instruction Reg.
X	1	0	Tach. Reg.
0	1	1	Checksum Reg.
1	1	1	Threshold Reg.

2. INSTRUCTION REGISTER. Stores 16-bit instruction word consisting of 6 bits of status information and 10 bits of instruction information.

3. DATA REGISTER. Stores 16-bit I/O data word that is to be written on or has been read from mag tape.

4. TACHOMETER REGISTER. Counts and stores both gap counts and tach pulses.

5. CHECKSUM REGISTER. Stores checksum calculated while reading or writing.

6. THRESHOLD REGISTER. Stores pre-compensation and one/zero threshold values.

7. WORKING REGISTER. Stores sum of data word and checksum that is to be written on tape.

8-51. TACO INSTRUCTION EXECUTION. When an instruction is not being executed, the TACO chip enters a "wait" mode and monitors the Holding Register. When the Holding Register has data in it, the TACO chip transfers this data to the appropriate register (e.g., Data, Instruction, or Threshold). If the data was an instruction word, execution of that instruction begins immeadiately. After the instruction is executed, the TACO chip returns to the wait mode.

8-52. INSTRUCTION/STATUS WORD FORMAT. The format of the instruction and status words is as follows:

I/O BIT	SIGNAL		STATE FUNCTIONS
0	HOL	S	1=Hole; 0=Not Hole
1	CIN	T	1=Cart. Out; 0=Cart. In
2	SFAIL	A	1=Servo Fail; 0=Servo OK
3	WPR	T	1=Write Protected; 0=Not Write Protected
4	GAP	U	1=In Gap; 0=Not In Gap
5	TRB	S	1=Select Track B; 0=Select Track A

6	MOD	I	1=High Volt Thres; 0=Low Volt Threshold
7	FST	N	1=90 ips; 0=22 ips
8	FGAP	S	1=Recognize Gaps > 1.5 in.
		T	0=Recognize Gaps > 0.066 in.
9	TDRON	R	1=Tape Drive ON; 0=Tape Drive OFF
10	G1	U--	
11	G2	C |	32 specific instructions governing:
12	G3	T |--	tape direction, speed, interrupt,
13	G4	I |	read/write mode, and erase.
14	G5	O--	
15	FWD	N	1=Forward; 0=Reverse

8-53. TACO STATUS. The 64000 system CPU is informed of TACO status via signals LFLG and LSTS on pins 28 and 29 of the I/O Data and Control Bus. LFLG is high when U9 is not selected and goes low when this chip is selected. LSTS is high when there are no controller or servo errors and goes low when an error occurs.

8-54. INTERRUPT REQUEST. When the TACO is ready to put data on the I/O data bus, signal LIR3 goes low and is fed to the interrupt circuitry on the 64000 system I/O circuit board and thence to the CPU circuit board.

8-55. SERVO CONTROL. The TACO chip provides for controlled acceleration and deceleration of the mag tape at 1200 ips within the velocity range of 2 to 90 ips. The servo uses frequency feedback signal FF to control the magnitude of error signals DA0 through DA5 and direction signal SIGN. There are 968 tach pulses for each inch of mag tape. Thus, at slow speed (21.98 ips) FF=2176 Hz. At fast speed (90.08 ips) FF=87196 Hz.

8-56. When stopping the tape, the servo controller uses a constant decleration to slow the tape down to 2 ips. At this point the TDRON signal clamps the drive signal to ground by turning on Clamp switch Q8. The drive signal remains grounded until the TACO chip is instructed to enter another mode. Conversely, when starting tape motion, the controller uses a constant acceleration until the tape speed reaches 2 ips. At this point the error signal becomes a function of Frequency Feedback signal FF. The error signal states are shown below:

ERROR SIGNAL STATES

CONDITION	SIGN	DA4	DA3	DA2	DA1	DA0
Stop FWD=1	1	0	0	0	0	0
Stop FWD=0	0	0	0	0	0	0
FWD, Initial Accel	0	0	1	1	0	0
REV, Initial Accel	1	0	1	1	0	0
FWD, Too Slow	0		ERROR			
FWD, Too Fast	1		ERROR			
REV, Too Slow	1		ERROR			
REV, Too Slow	0		ERROR			

Table 8-3. TAPE CONTROLLER U9 I/O SIGNALS

MNEMONIC	COMMON NAME	ACTIVE STATE	CHARACTERISTIC AND FUNCTION
BD	Bus Drive	Low	Output; open collector; when low TACO chip is driving the I/O Data Bus.
CIN	Cartridge In	High	Input; when high indicates that tape cartridge is inserted.
CLK	Clock	----	Input; clock input to U9; 4 MHz squarewave.
DA(0-4)	Digital-to-Analog Error Signal	High	Output; 5V active pullup; provides binary count to D/A convertor indicating error magnitude of transport motor speed. DA0=LSB
DOUT	Data Out	Low	Input; indicates direction of data flow; 0= write into U9; 1=read from U9 (if U9 is selected).
FF	Frequency Feedback	----	Input; tach pulse used for controlling drive motor speed and detecting gaps. 968 pulses are generated for each inch of tape.
FLG	Flag	Low	Output; open collector; goes low when U9 is selected (STSEN must also be low and no error conditions can exist).

FR	Flux Reversal	High	Input; indicates that a flux reversal has been detected by the read circuits; this signal is recognized only after a low-to-high transition of THR; FR is used during read to time bit lengths and for gap detection when tape speed is less than 22 ips.
FST	Fast	High	Output; 5V active pullup; when high, sets high voltage threshold for flux reversal detection at fast speed; when high, tape speed=90 ips; when low, speed=22 ips.
HOL	Hole	High	Input; when high indicates that a hole has been detected on the mag tape.
IC1,2	Interface Commands	Low	Input; these signals select a specific U9 register to be read or written.
INIT	Initialize	Low	Input; goes low at power turn-on to intialize U9; remains low until power supplies and clock have stabilized.
INT	Interrupt	Low	Input; goes low to indicate that CPU has requested an interrupt poll.
IOD0-5	I/O Data	Low	Input-output; 5V active pullup; 16 data signals that are used for communicating with U9 registers.

IOSB	I/O Strobe	Low	Input; when low strobes data into U9 registers; data is latched on positive-going edge; also is CPUs answer to U9 when interrupt is re-request-
IR	Interrupt Request	Low	Output; open collector; goes low when U9 is requesting interrupt from CPU; remains low until IOSB occurs.
LTCH	Latch	Low	Input; when low latches current state of PAD-3 and IC1,2.
MOD	Mode	High	Output; when high selects high threshold for flux reversal dection when either MOD instruction bit is active or when both a gap and slow speed (22 ips) occurs.
PA0-3	Peripheral Address	Low	Input; U9 is selected when all four signals are low.
PACK	Poll Acknowledge	Low	Output; open collector; goes low to acknowledge interrupt poll when INT=0, PA3=0, and U9 is requesting an interrupt.
SFAIL	Servo Fail	Low	Input; goes low to indicate the servo has failed.
SIGN	Sign-of-Error	High	Output; 5V active pullup; changes polarity to indicate if motor speed is too fast or too slow.

STS	Status	Low	Output; open collector; goes low to indicate lack of error condition (U9 must be selected and STSEN must be low).
STSEN	Status Enable	Low	Input; goes low to enable STS and FLG signals.
TDRON	Tape Drive On	High	Output; open collector; goes high to indicate (via front panel lamp) that tape drive is on; goes low to prevent drive motors from creeping when speed is less than 2 ips.
TEST	Test	Low	Input; serves as additional address bit (with IC1,2) to access various internal registers for test purposes.
THR	Threshold	High	Input; when high indicates that the playback signal is above a specified threshold of bit length. Used for detecting gaps when tape speed is greater than 22 ips.
TRB	Track B	High	Output; 5V active pullup; when high causes track B to be selected; when low selects track A.
WDT	Write Data	High	Output; open collector; comprises data to be recorded.
WPR	Write Protect	High	Input; goes high to prevent writing on tape when cartridge is in write protect mode.
WRT	Write	High	Output; open collector; when high provides write current to record head.

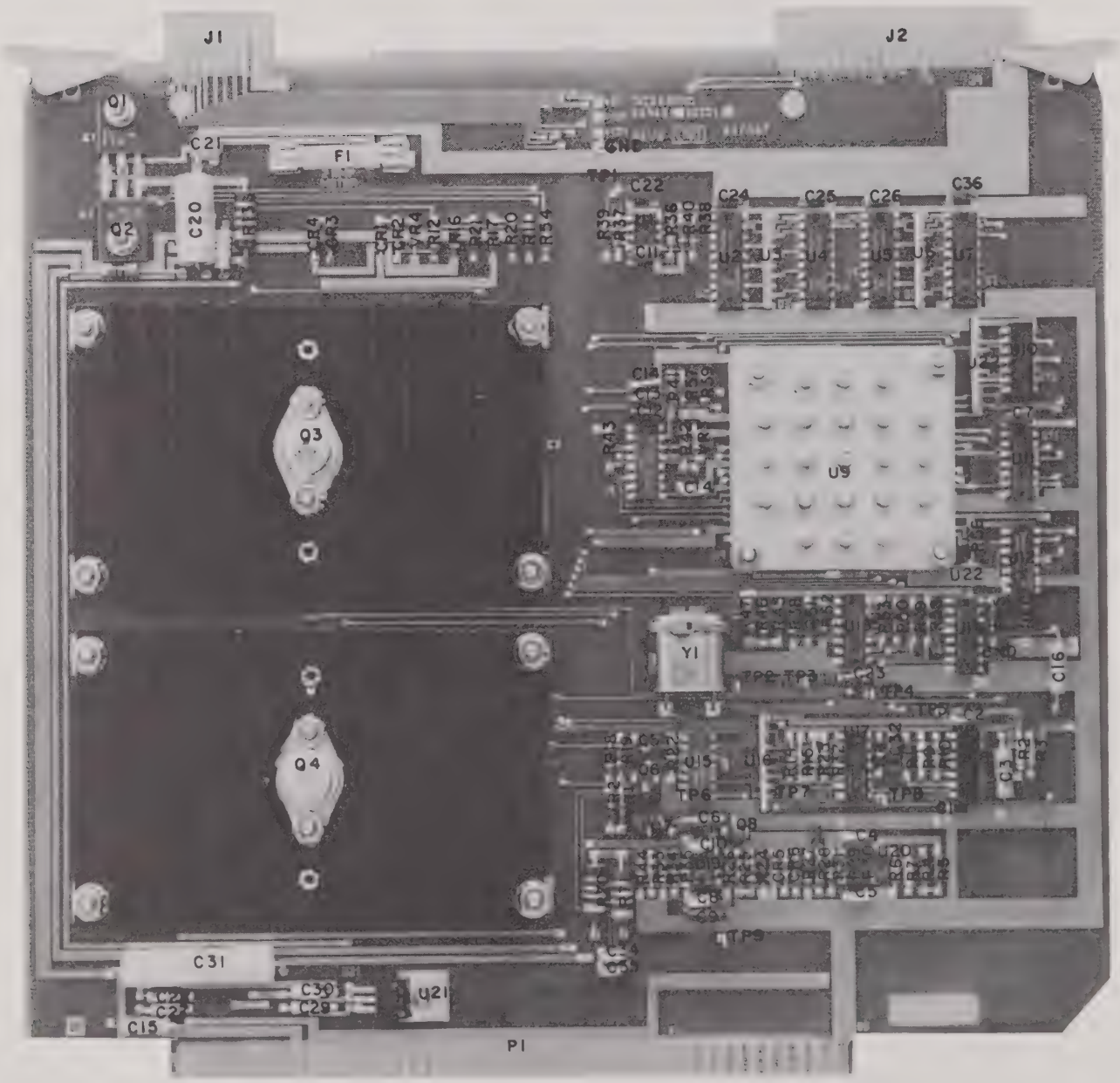
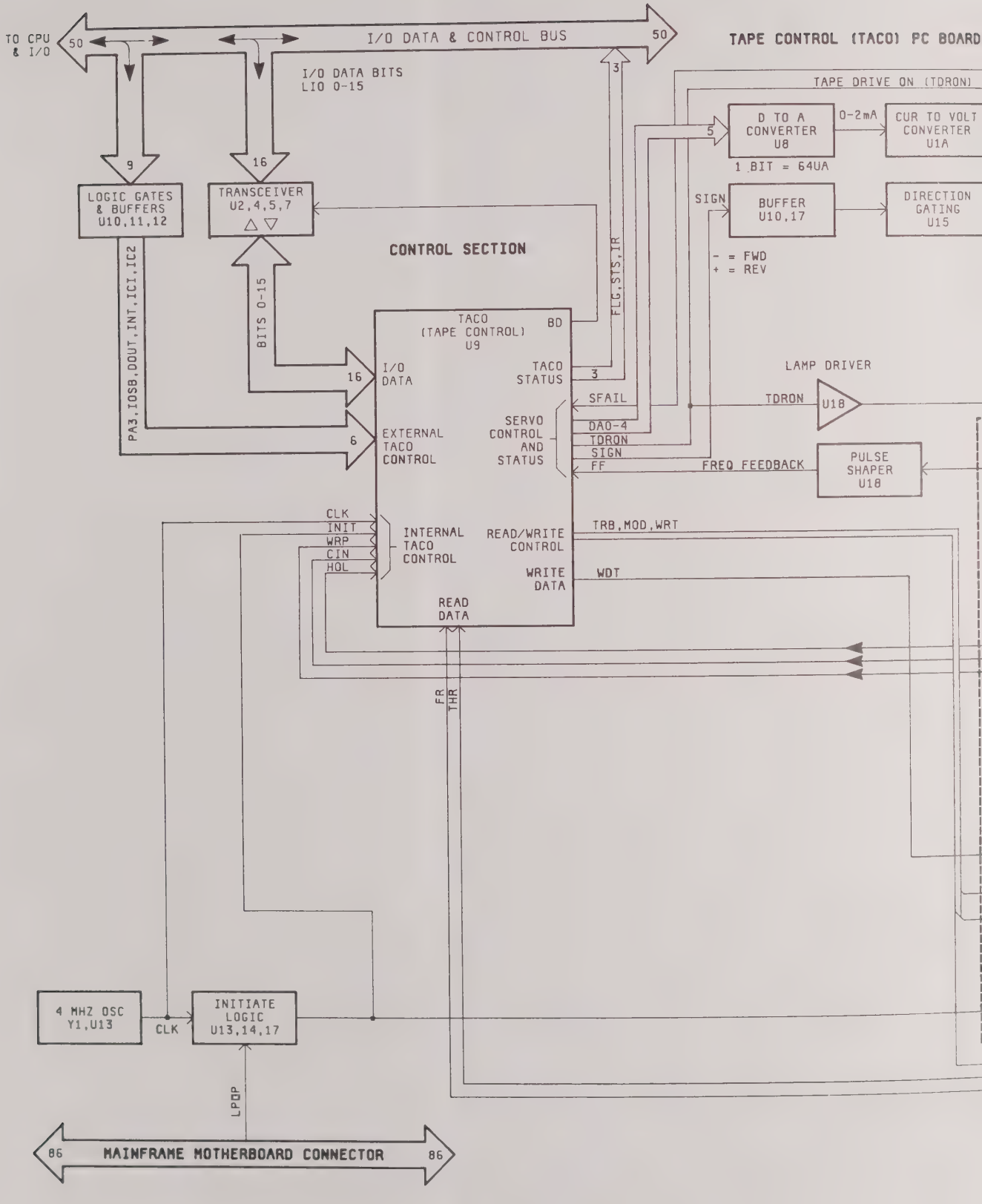
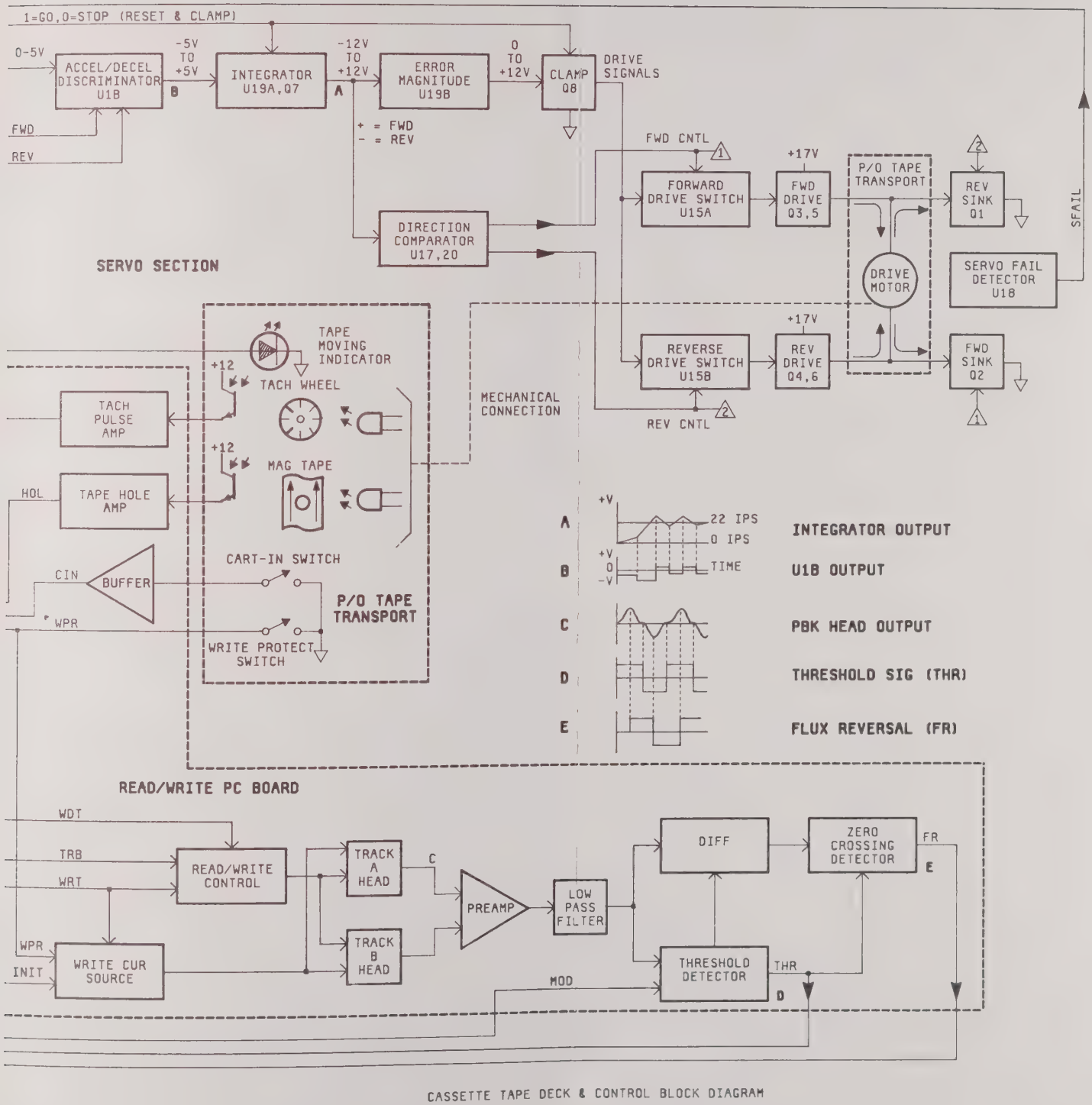


Figure 8-1. Tape Controller PCB Component Locator

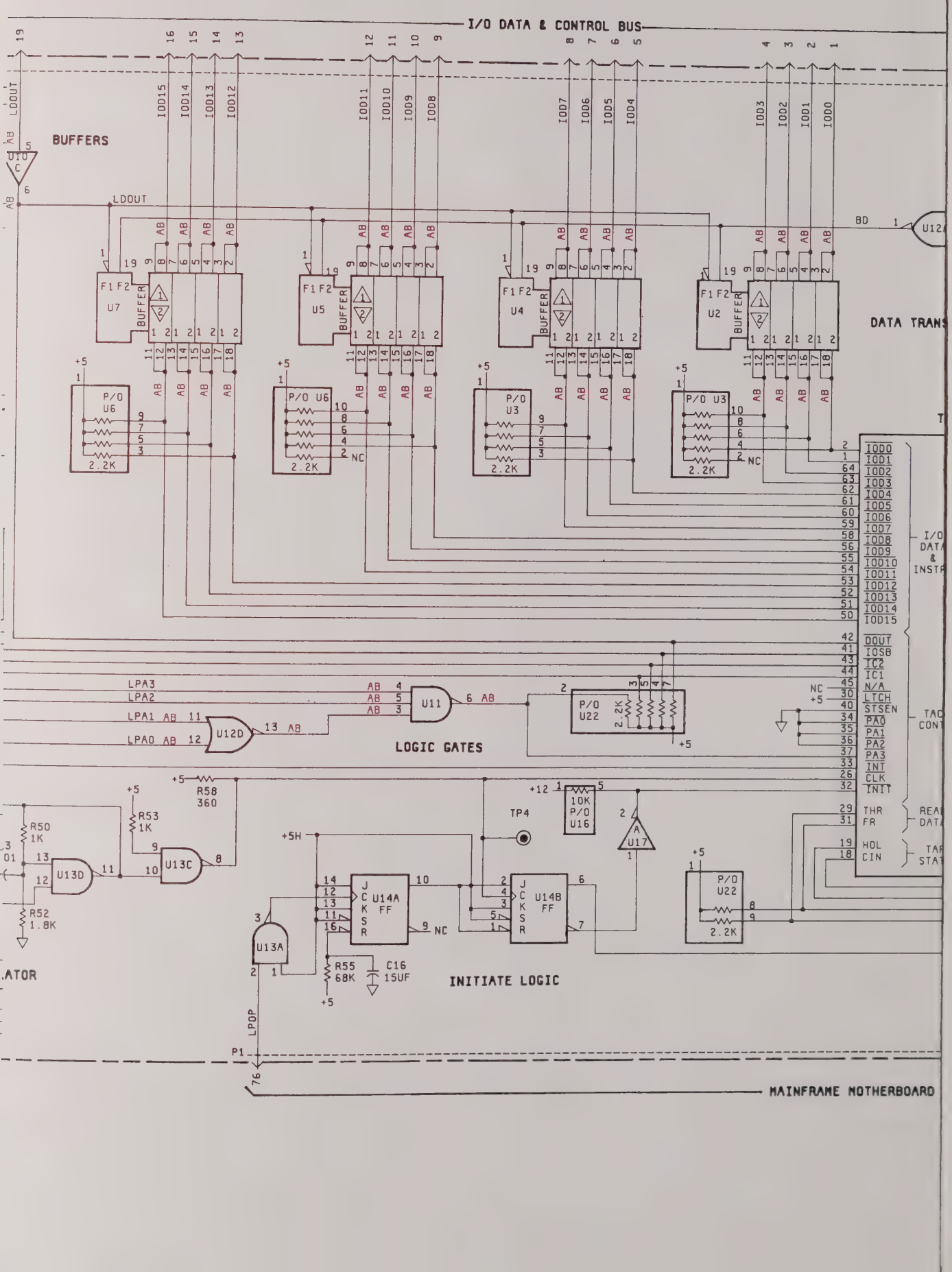

TAPE CONTROL (TACO) PC BOARD
TO CPU & I/O
50
I/O DATA & CONTROL BUS
50
I/O DATA BITS LIO 0-15
3
TAPE DRIVE ON (TDRON)
5
D TO A CONVERTER U8
0-2mA
CUR TO VOLT CONVERTER U1A
1 BIT = 64UA
SIGN
BUFFER U10,17
DIRECTION GATING U15
- = FWD
+ = REV
9
16
LOGIC GATES & BUFFERS U10,11,12
TRANSCEIVER U2,4,5,7
CONTROL SECTION
BITS 0-15
PA3,IOSB,DOUT,INT,ICI,IC2
FLG,STS,IR
TACO (TAPE CONTROL) U9
BD
I/O DATA
16
TACO STATUS
3
SFAIL
LAMP DRIVER
TDRON
U18
SERVO CONTROL AND STATUS
DA0-4
TDRON
SIGN
FF
FREQ FEEDBACK
PULSE SHAPER U18
EXTERNAL TACO CONTROL
6
CLK
INIT
WRP
CIN
HOL
INTERNAL TACO CONTROL
READ/WRITE CONTROL
TRB,MOD,WRT
WRITE DATA
WDT
READ DATA
FR
THR
4 MHZ OSC Y1,U13
CLK
INITIATE LOGIC U13,14,17
LPOP
86
MAINFRAME MOTHERBOARD CONNECTOR
86



CASSETTE TAPE DECK & CONTROL BLOCK DIAGRAM

Figure 8-2. Tape Cassette System Block Diagram

TAPE CONTROL (64940-66501)
J2
26
21
22
23
24
17
18
25
LINT
LPA0
LPA1
LPA2
LPA3
LIC1
LIC2
LIOSB
AB
U10
A
B
F
1
2
3
4
13
12
6
P/O
U22
2.2K
1
+5
Y1 XTAL
4 MHZ
R49
1K
5
U13B
6
4
R48
1.8K
R51
1K
+5
4MHZ OSCIL


I/O DATA & CONTROL BUS
BUFFERS
LDOUT
IOD15
IOD14
IOD13
IOD12
IOD11
IOD10
IOD9
IOD8
IOD7
IOD6
IOD5
IOD4
IOD3
IOD2
IOD1
IOD0
U7
U5
U4
U2
BUFFER
P/O U6
P/O U3
P/O U22
2.2K
NC
DATA TRANS
I/O DATA & INSTR
LPA3
LPA2
LPA1
LPA0
U11
U12D
LOGIC GATES
R58 360
R53 1K
R50 1K
R52 1.8K
U13D
U13C
U13A
U14A FF
U14B FF
10K P/O U16
U17
TP4
+5H
R55 68K
C16 15UF
INITIATE LOGIC
LPOP
P1
MAINFRAME MOTHERBOARD

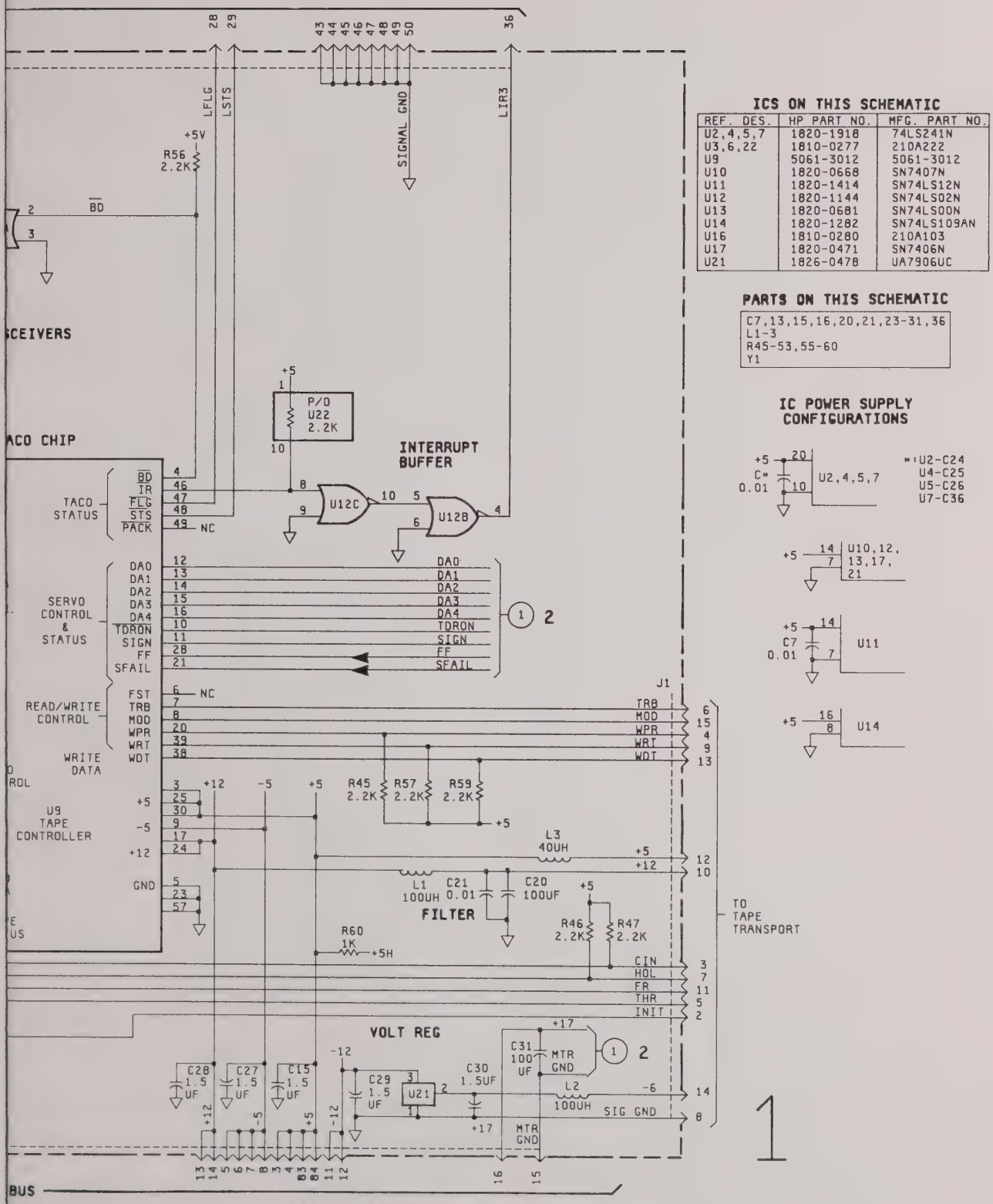
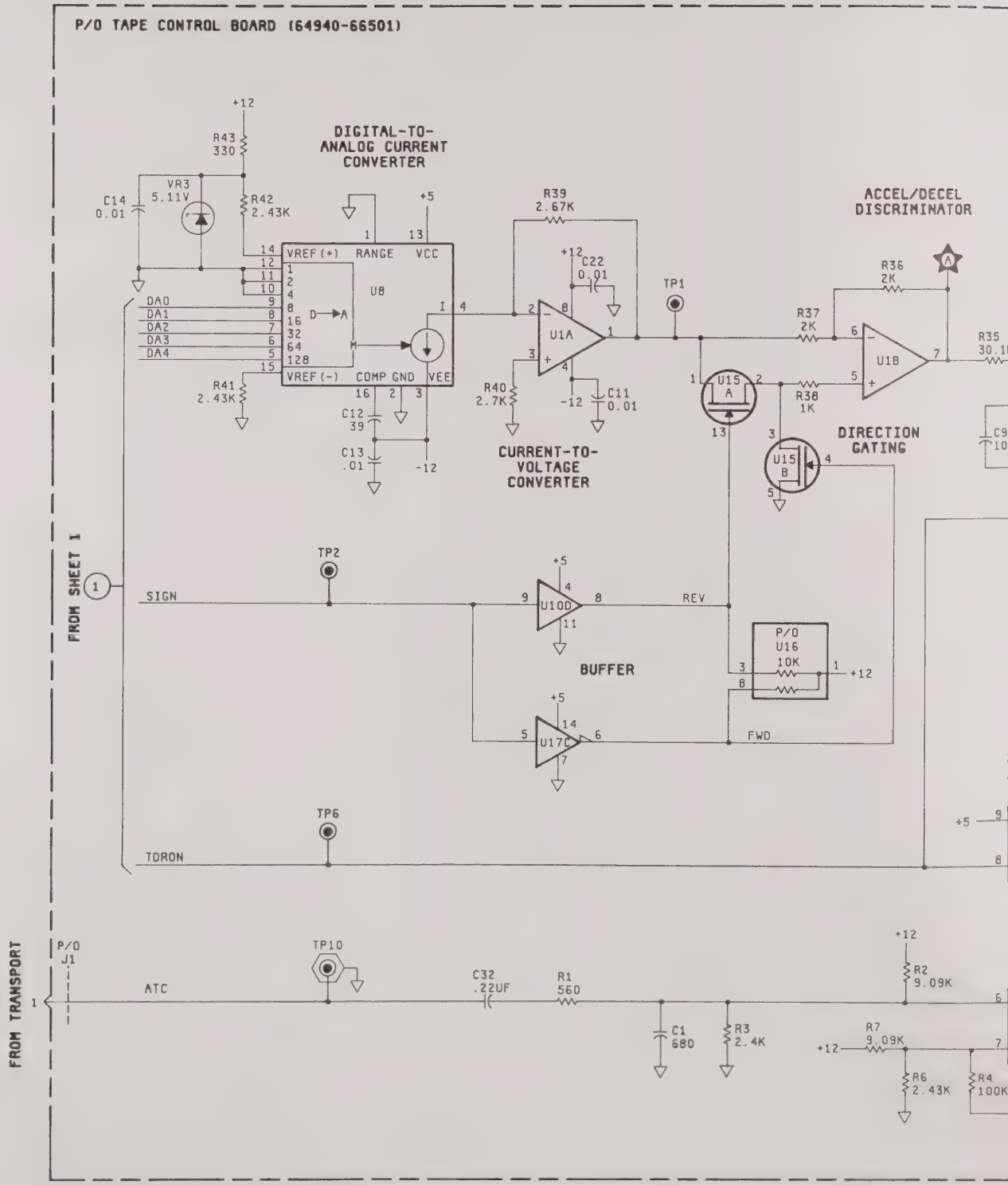


Figure 8-3. TAPE CONTROL SCHEMATIC (SHEET 1 OF 2)

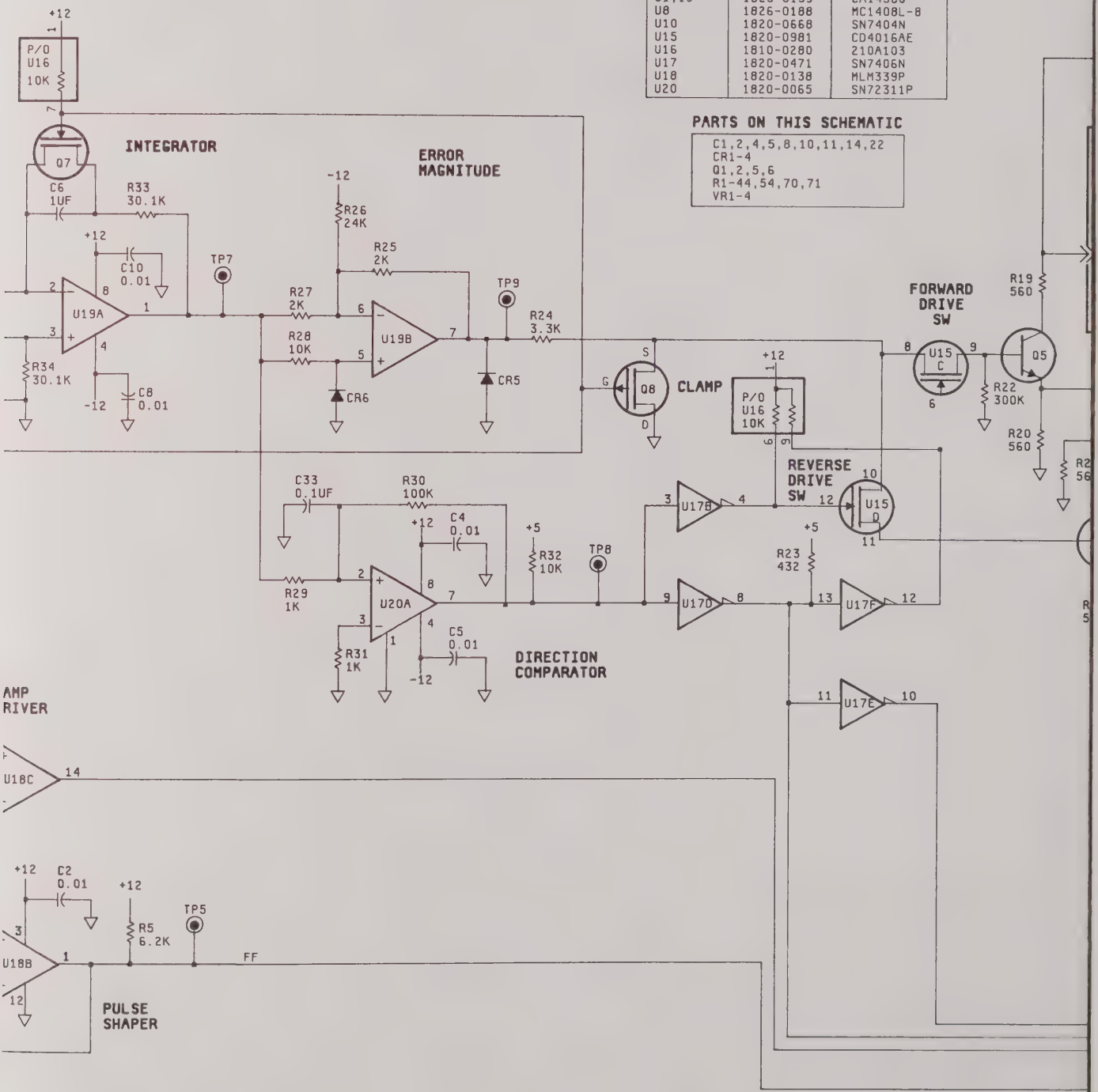

P/O TAPE CONTROL BOARD (64940-66501)
DIGITAL-TO-ANALOG CURRENT CONVERTER
CURRENT-TO-VOLTAGE CONVERTER
ACCEL/DECEL DISCRIMINATOR
DIRECTION GATING
BUFFER
FROM SHEET 1
FROM TRANSPORT
SIGN
TDRON
REV
FWD
ATC
U8
U1A
U1B
U15 A
U15 B
U10D
U17C
P/O U16 10K
VR3 5.11V
R43 330
R42 2.43K
R41 2.43K
R39 2.67K
R40 2.7K
R37 2K
R36 2K
R38 1K
C14 0.01
C22 0.01
C11 0.01
C12 39
C13 .01
C32 .22UF
R1 560
C1 680
R3 2.4K
R2 9.09K
R7 9.09K
R6 2.43K
R4 100K
TP1
TP2
TP6
TP10
P/O J1
DA0
DA1
DA2
DA3
DA4
VREF(+)
VREF(-)
RANGE
VCC
COMP
GND
VEE
+12
+5
-12

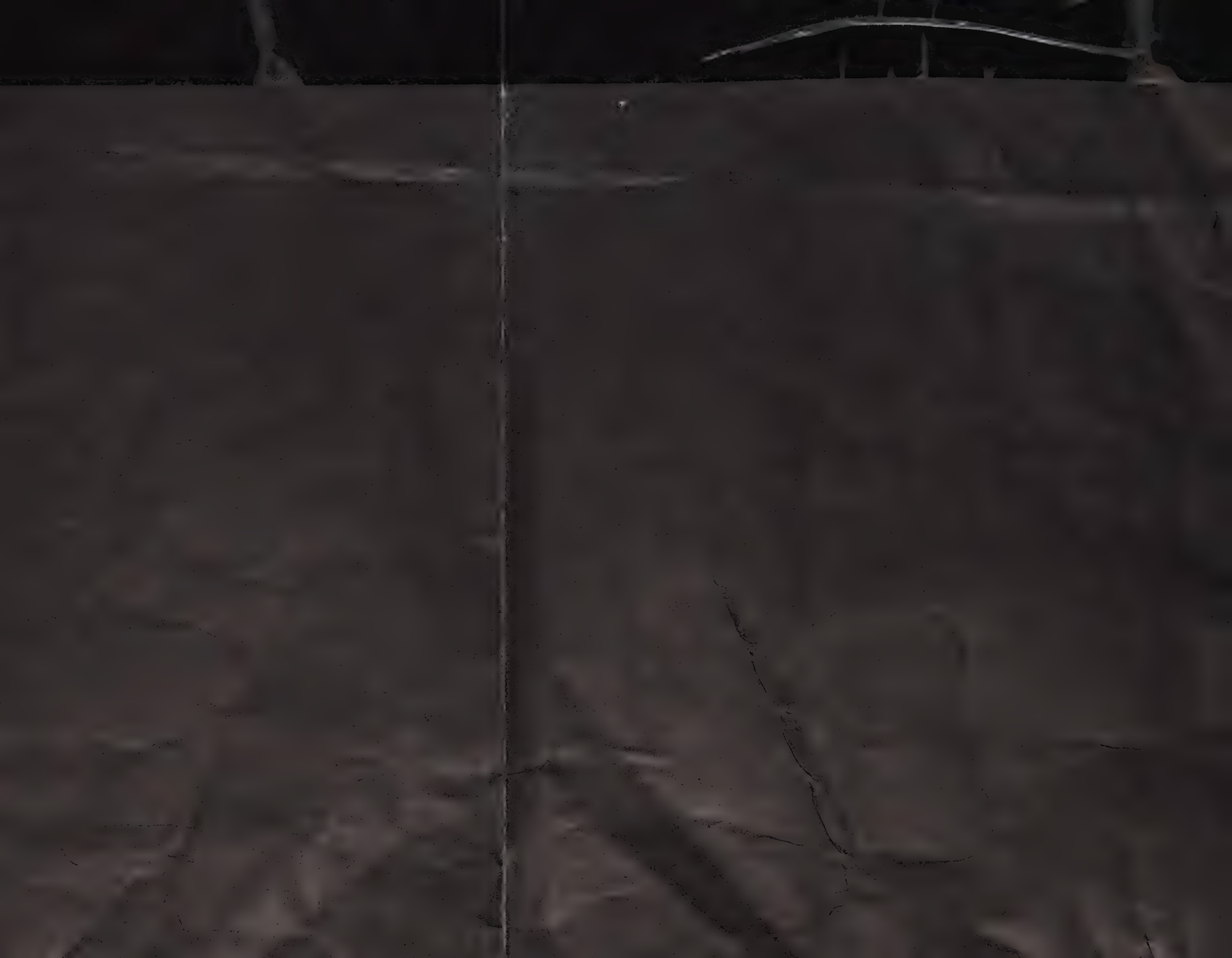
ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U1,19	1826-0139	CA1458G
U8	1826-0188	MC1408L-8
U10	1820-0668	SN7404N
U15	1820-0981	CD4016AE
U16	1810-0280	210A103
U17	1820-0471	SN7406N
U18	1820-0138	MLM339P
U20	1820-0065	SN72311P

PARTS ON THIS SCHEMATIC

C1,2,4,5,8,10,11,14,22
CR1-4
Q1,2,5,6
R1-44,54,70,71
VR1-4





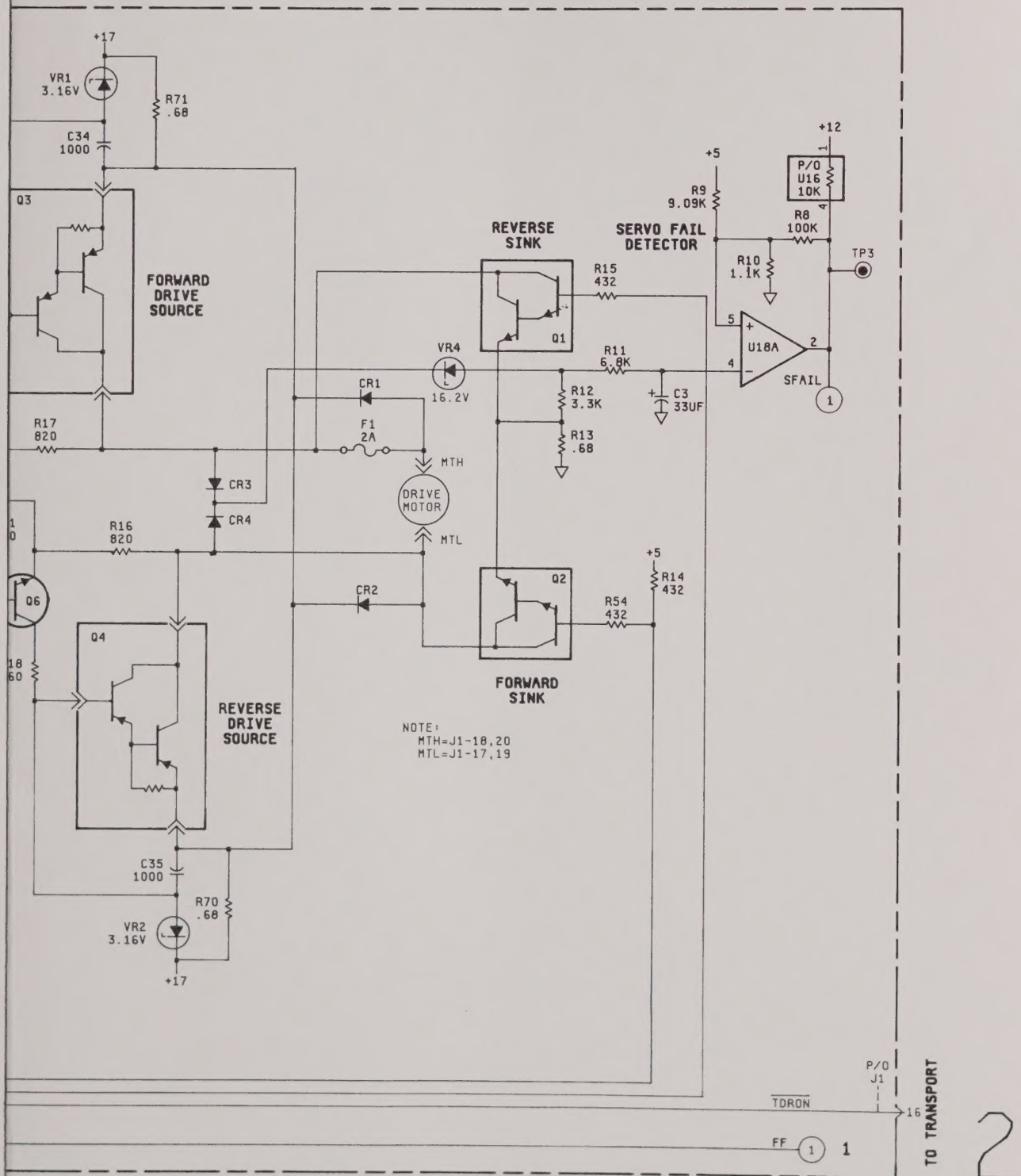


Figure 8-3. Tape Controller Schematic (sht 2 of 2)

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